Docket No.: M4065.0107/P107-F
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Howard E. Rhodes et al.

Application No.: 10/761,319 | Confirmation No.: 2671

Filed: January 22, 2004 | Art Unit: 2622

For: TWIN PWELL WITH A RETROGRADE PWELL FOR CMOS IMAGERS | Examiner: Chia Wei A. Chen

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

As required under 37 C.F.R. § 41.37(a), this brief is filed within three months of the Notice of Appeal filed in this case on October 16, 2008, with payment of the requisite fee for a one-month extension of time and is in furtherance of said Notice of Appeal. A one-month extension of time for filing is respectfully requested.

The fees required under 37 C.F.R. § 41.20(b)(2) are submitted herewith and are identified in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Aptina Imaging Corporation, a corporation of the Cayman Islands, and the assignee of this application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 21 claims pending in application. A listing of the claims is attached hereto in the Claims Appendix.

B. Current Status of Claims

1. **Claims canceled: 1-69 and 80-119.**
2. **Claims withdrawn from consideration but not canceled: none.**
3. **Claims pending: 70-79 and 120-130.**
4. **Claims allowed: none.**
5. **Claims rejected: 70-79 and 120-130.**

C. Claims On Appeal

The claims on appeal are claims 70-79 and 120-130.

IV. STATUS OF AMENDMENTS

After the final rejection, Applicants filed a Response to Final Action under 37 C.F.R. § 1.116 with no amendment to the claims. There has been no amendment to the claims since the final rejection. Separate from the filing of this Appeal Brief (on January 12, 2009) Applicants filed a Terminal Disclaimer with respect to U.S. Patent No. 6,310,366 to Rhodes et al. A copy of the Terminal Disclaimer is attached at Appendix B. The Terminal Disclaimer should overcome the rejection of claims 70-79 and 120-130 on the ground of obviousness-type double patenting, as discussed below.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Introduction

This application is a divisional application of U.S. Application Ser. No. 10/295,952 (now U.S. Patent No. 6,787,818), which is a continuation of U.S. Application Ser. No. 09/918,450 (now U.S. Patent No. 6,483,129), which is a divisional of U.S. Application Ser. No. 09/334, 261 (now U.S. Patent No. 6,310,366, the original case in the family). The priority date for this application is June 16, 1999. Other related patents claiming priority to the same original filing are U.S. Patent Nos. 6,445,014; 6,686,220; and 6,858,460.

The invention is directed generally to semiconductor imagers incorporating a retrograde well in the substrate below a pixel array. Published Application No. US 2004/0150736 Abstract; ¶0024.[1] The pixel array converts light energy into electrical signals and is used to generate images in devices such as digital cameras. The invention is non-exclusively applicable to imager pixel arrays, for example, CMOS (complementary metal oxide semiconductor) imager pixel arrays formed over a substrate (16) and a surface well (20) (Fig. 5). A photosensor (a photosite) such as photogate or photodiode is formed within each pixel for generating charges corresponding to received light at the pixels, which may also include circuitry (26, 28, 29, 30, 31, 32, 34, 36, 38, 39, 40, 42, 44) for transferring the photogenerated-signal out of the pixel and resetting the pixel. *Id.* ¶¶0008-21.

In imager applications, charge loss is a problem because of the leakage of signal carriers out of one pixel and into the underlying substrate or into an adjacent pixel. *Id.* ¶0022. This can result in decreased signal strength, increased cross-talk between pixels, and the incorrect reading of the pixels. *Id.* ¶¶0022-23. The claimed devices with the recited retrograde well structure provides better efficiency, improved signal-to-noise ratio, and reduced cross-talk by reflecting charge carriers at the well/substrate interface and reducing charge leakage. *Id.* ¶¶0023-24.

The recited retrograde well structure, over which an array of pixels is provided, has a dopant region with a vertically graded dopant concentration that is lowest at the substrate surface and highest at the bottom of the well. *Id.* ¶0024; Fig. 6. The retrograde well reflects charges back to the photosensors of the pixels so charges are not lost to the substrate, which provides the sought-after advantages identified above. *Id.* An example of such a structure is shown in Fig. 5 of the application where the retrograde well is identified as number 20. *Id.* ¶¶0040-44. Fig. 5 (annotated) from the Application is reproduced below:

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[1] Citations herein to the application are to the specification of the published application, which has paragraph numbering, unless otherwise indicated. For the Board's convenience, a copy of the published application is provided herewith at Appendix D.

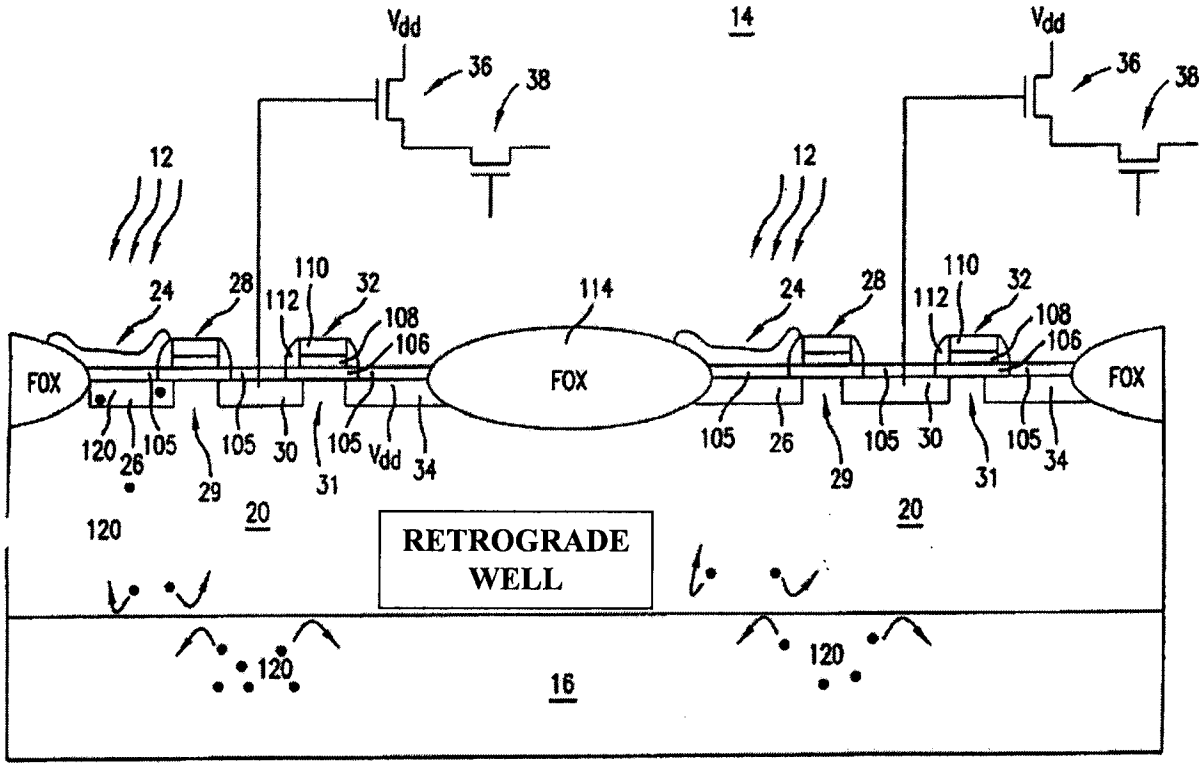


FIG.5

As illustrated by Fig. 5, electrical carriers (120) generated from light radiation (12) at a photosensor (26), in the retrograde well (20), and are stored as electrons. *Id.* ¶0044; Fig. 5. The retrograde well (20) acts to reduce carrier (120) loss to the underlying substrate (16) by forming a concentration gradient that modifies the band diagram and serves to reflect electrons escaping from the pixel back to the photosensor (26). *Id.* ¶0044. The retrograde well (20) also acts to reflect charges (120) from within the substrate (16) back into the substrate to keep them from entering the retrograde well (20) and thus being received by the photosite (26) within the well (20). These charge reflections improve quantum efficiency of the pixels. *Id.*

B. Summary of Subject Matter of Claim 70

Independent claim 70 defines an imager device. This device includes (Figs. 5 and 11) an array (442) of pixel sensor cells (14) formed in a retrograde well (20) on a substrate (16), the retrograde well (20) being doped with a vertically graded dopant profile (Fig. 6), wherein each pixel sensor cell (14) has a photosensitive region (26) and a photosensor (24) formed at the photosensitive region (26). *Id.* ¶¶0040-44, 0051. The device further includes a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image. *Id.* ¶0042. Also, the device includes a processor (444) for receiving and processing data representing the image. *Id.* ¶¶0050-51. The reference numbers identified are representative and the claim should not be interpreted as incorporating specific embodiments into the claims.

C. Summary of Subject Matter of Claim 120

Independent claim 120 defines a CMOS imager device, which includes (Fig. 5) an array of pixel sensor cells (14) formed in a retrograde well (20) in a substrate (16), the retrograde well (20) being doped with a vertically graded dopant concentration (Fig. 6), wherein each of the pixel sensor cells (14) is separated by an isolation region (114) that electrically isolates the pixel cells (14) from each other. *Id.* ¶¶0040-44. Further, each pixel sensor cell has a photoconversion device (24), a reset transistor (31), a source follower transistor (36), a row select transistor (38), and a floating diffusion region (30) in electrical communication with said photoconversion device (24) and said source follower transistor (36). *Id.* ¶¶0011-12 and 0040-45. The reference numbers identified are representative and the claim should not be interpreted as incorporating specific embodiments into the claims.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 70-79 are unpatentable on the ground of nonstatutory obviousness-type double patenting over claims 36-45 of U.S. Patent No. 6,310,366 ("Rhodes et al.").

B. Whether claims 120-130 are unpatentable on the ground of nonstatutory obviousness-type double patenting over claims 20-35 of Rhodes et al. in view of U.S. Patent No. 5,471,515 ("Fossum").

C. Whether claims 70, 120, and 122-124 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,859,450 ("Clark") in view of U.S. Patent 4,578,128 ("Mundt").

D. Whether claims 71-79 and 125-130 are unpatentable under 35 U.S.C. § 103(a) over Clark in view of Mundt and further in view of U.S. Patent No. 6,093,951 ("Burr").

E. Whether claim 121 is unpatentable under 35 U.S.C. § 103(a) over Clark in view of Mundt and further in view of U.S. Patent No. 6,657,665 ("Guidash").

VII. ARGUMENT

The Grounds of Rejection set forth above are based on a final rejection made by the Examiner in an Office Action dated May 16, 2008. Applicants responded to this Office Action on August 15, 2008, without amending the claims. An Advisory Action was mailed September 26, 2008, indicating (at 2) that the rejections over the prior art were sustained and that the finality of the May 16, 2008, Office Action would not be withdrawn. Applicants filed a Notice of Appeal, with the requisite fee, on October 16, 2008. This brief is timely filed with a request for extension of time and the requisite fee.

A. Claims 70-79 are patentable over claims 36-45 of Rhodes et al. in view of the filed terminal disclaimer.

On January 12, 2009, Applicants filed a terminal disclaimer with respect to Rhodes et al. Accordingly, this double patenting rejection is now moot.

B. Claims 120-130 are patentable over claims 20-35 of Rhodes et al. in view of Fossum in view of the filed terminal disclaimer.

On January 12, 2009, Applicants filed a terminal disclaimer with respect to Rhodes et al. Therefore, this double patenting rejection is moot.

C. Claims 70, 120, and 122-124 would not have been obvious under 35 U.S.C. § 103(a) over Clark in view of Mundt. Even if combinable, the references fail to teach or suggest each element of the claims. The references, however, are not properly combinable because they at least teach away from such combination and would make for a seemingly inoperable device according to the primary reference. There is no reason to combine the references and the Final Rejection fails to make a *prima facie* case for doing so.

Claim 70 defines an imager and recites "an array of pixel sensor cells formed in a retrograde well on a substrate, the retrograde well being doped with a vertically graded dopant profile, wherein each pixel sensor cell has a photosensitive region and a photosensor formed at the photosensitive region; a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image; and a processor for receiving and processing data representing the image." Such a device would not have been obvious over Clark in view of Mundt.

1. The Clark-Mundt Combination Fails To Teach Or Suggest Each Element Of Independent Claim 70

The Final Rejection's argument for unpatentability indicates (at 4) that Clark teaches a pixel array, a circuit, and a processor according to independent claim 70. However, the Final Rejection specifically acknowledges that Clark does not teach a retrograde well on a substrate doped with a vertically graded dopant profile, as recited by claim 70. The Final Rejection is correct, Clark does not disclose a retrograde well as a part of its structure. In fact, in addition to not disclosing a retrograde well, Clark also does not teach "an array of pixel sensor cells formed in a retrograde well," as recited by claim 70. All Clark teaches is a respective well (206) at each photosite location, which is different than a well, retrograde or not, below an array of photosites.

There is no disclosure of an array of pixel cells formed in a well. There is no disclosure of how a single well can mitigate charge loss for an array of pixels.

Clark does not recognize that charge loss to, or unwanted charge migration into pixels from, the bottom part of the substrate can be a problem, thus it fails to identify any need for incorporating a vertically graded retrograde well with a photodiode array and it certainly does not disclose an array of cells formed in a retrograde well. While Clark fails to recognize the specific charge loss problems improved by the presently clamed invention it nevertheless identifies that the problem it intends to mitigate is charge leakage at the substrate surface from an individual photosensor cell. Clark indicates that charge leakage from a cell is mitigated, dark current reduced, and signal-to-noise ratio improved by providing a heavily doped region (HDR) guide ring (220) at the substrate surface surrounding each photosensitive region. Clark col. 3, ll. 30-42; col. 4, ll. 14-20; col. 5, ll. 1-7; Figs. 2 and 5b. Thus, Clark provides a structure (the guard ring 220) for each photosite, which is different than the recited "array of pixel sensor cells formed in a retrograde well," which prevents charge leakage into the substrate (as well as into the array from the substrate). Clark has no recognition of, nor a solution for, charge loss into the substrate or charge contamination from charges within the substrate for an array of pixel cells within a retrograde well.

For disclosure of a retrograde well, the Final Rejection (at 5) turns to Mundt, identifying features 52P, 52N of Fig. 8 (Mundt col. 5, ll. 27-33) as the recited retrograde well, which is absent from Clark. Mundt is not directed to and does not disclose an imager, but instead discloses a CMOS integrated (logic) circuit comprising a PMOS FET (a p-channel field effect transistor) and an NMOS FET (an n-channel field effect transistor). Mundt discloses using a retrograde well to reduce latchup for an individual transistor in this device and to make it compatible with trench isolation structures. Mundt col. 4, ll. 3-15; col. 5, ll. 8-36. While Mundt discloses a retrograde well for an individual transistor, it does not address the problem of charge loss from a pixel array or the need for charge reflection at the interface between a well beneath a pixel array and a substrate in an imager. For this reason alone, the retrograde well of Mundt

would not have been combined by one skilled in the art with the photosensor structure of Clark. There is simply nothing in either reference to suggest that the Mundt structure would have any utility or solve a problem in the Clark imager. Moreover, even when combined with Clark, there still remains no teaching or suggestion for an array of pixel cells formed within a retrograde well.

Thus, even if the Clark and Mundt references were properly combinable, which they are not for the multiple reasons discussed below, the combination would still not teach or suggest "an array of pixel sensor cells formed in a retrograde well on a substrate," as recited by claim 70. Mundt does not disclose that its retrograde well can be used with even a single pixel sensor cell, much less under an array of such cells. Clark's charge leakage control ring (220) is a structure disclosed as used with and around the photosensors of individual pixels and not as a single formation below an entire array of cells. Accordingly, the Clark-Mundt combination fails to teach or suggest each feature of the claimed subject matter and the rejection should be reversed for this reason.

2. Clark And Mundt Would Not Have Been Combined Because They Relate To Different Semiconductor Devices With Different Problems To Solve

As for reasoning to combine Clark and Mundt to arrive at the claimed subject matter, the Final Rejection (at 5; *see also*, Advisory Action at 4-5) merely indicates that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the retrograde doped substrate with the imager of Clark since retrograde dopant distribution in semiconductor substrates have the potential of increased device packing density and decreased susceptibility to latchup" (citing Mundt col. 1, ll. 15-20). Latchup is a condition when transistors or other integrated circuit devices turn on and cannot be turned off – a short circuit. *See, e.g.*, Latchup – Wikipedia, http://en.wikipedia.org/wiki/Latchup; and Latch-Up in CMOS Designs, http://www.ece.drexel.edu/courses/ECE-E431/latch-up/latch-up.htm (each attached at Appendix B). This condition has no applicability to the pixel array of the present claims, but even if it did, Mundt would only teach one retrograde well per transistor. Mundt would not teach or suggest the use of a retrograde well in which an array of pixel cells are formed or even the use of a

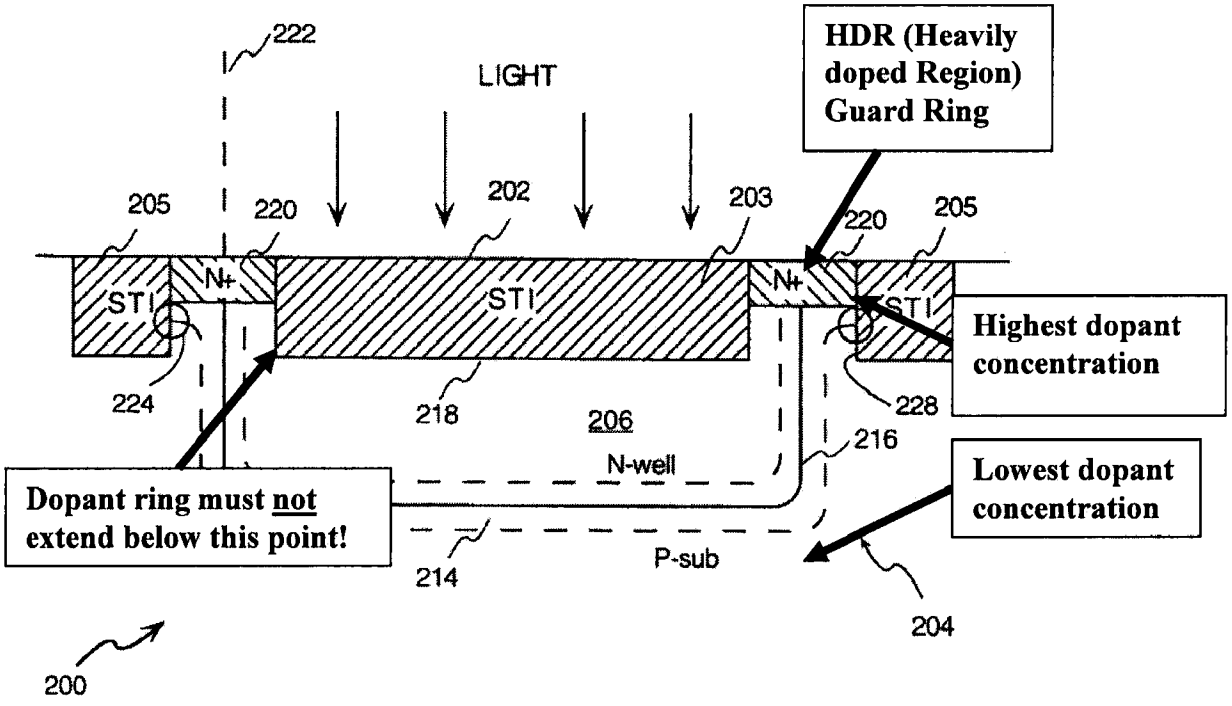
retrograde well with a photosensor. Thus, the recognition of benefits of preventing transistor latchup in Mundt would not apply to the Clark photosensor.

There is no evidence of record that the photosensors of Clark are subject to a "latchup" problem as addressed by Mundt. Therefore, there is no motivation to use the Mundt retrograde well in Clark. The Final Rejection fails to establish otherwise and lacks a *prima facie* case for obviousness, which is the examiner's burden. *In re Fritch*, 972 F.2d 1260 (Fed. Cir. 1992) (finding no motivation to combine merely because the prior art could be modified to meet the invention). Having failed to meet this burden, the rejection should be reversed.

3. There Would Have Been No Motivation To Combine Clark And Mundt Because The References Teach Away From Such Combination, The Combination Would Leave The Primary Reference Seemingly Inoperable, And The Primary Reference Already Deals With Similar Problems To That Addressed By The Present Invention In A Different Way

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless . . . the results would have been predictable to one of ordinary skill in the art." M.P.E.P. § 2143.01 (emphasis original) (citing *KSR International Co. V. Teleflex Inc.*, 550 U.S. __, __, 82 USPQ2d 1385, 1396 (2007)). If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *Id.* (citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)). "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." M.P.E.P. § 2141.02 (citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). "'When the prior art **teaches away** from combining certain known elements, discovery of successful means of combining them is **more likely to be nonobvious**.'" M.P.E.P. § 2143 (quoting *KSR Int'l*, 127 S.Ct. at 1740, 82 USPQ2d at1395) (emphasis added).

Although Clark discloses a photosensor and Mundt discloses a retrograde well for complementary PMOS and NMOS FETs, these references are not properly combinable under 35 U.S.C. § 103(a) because there would have been no motivation to do so. The present application identifies the advantages of including the recited "retrograde well being doped with a vertically graded dopant profile" with an array of pixel cells as the repelling of signal carriers from the photosensors so they are not lost to the substrate and reducing noise by preventing carriers from the substrate from diffusing up into the photosensor. Clark identifies similar needs as being already met by its disclosed invention – minimizing dark current, reducing current leakage, and reducing noise (Clark col. 1, ll. 27-43) – these identified needs are met by providing a guard ring (220) at the substrate (204) surface around each of the individual photosensitive regions of the sensor cells at an STI (shallow trench isolation) region (202) (*id.* col. 3, l. 30 to col. 4, l. 20). Fig. 2 from Clark, illustrating this guard ring, is reproduced (annotated) below:



The guard ring (220) of Clark is a **surface** feature of its photosensor that is a heavily doped substrate region that surrounds the photosensor (feature 214 is a depletion region where

photocharge is generated). Clark also discloses a dopant well (206) below the photosensor and the guard ring (220). Clark specifically indicates that its invention, i.e., the guard ring (220), satisfies its indicated purpose, i.e., it "contributes to a decrease of the dark current in the embodiment of the photodiode according to the present invention," because the substrate doping is graded so that it has a higher doping near the surface – the opposite of a retrograde well, which has lower dopant concentration at the surface and higher dopant concentration at depth. Clark col. 4, ll. 13-20. It is **absolutely essential** to the invention of Clark that its disclosed dopant, provided as ring (220), have a higher concentration at the substrate surface, as explained below. It cannot be retrograde. This is exactly the opposite of the Mundt retrograde well.

According to M.P.E.P. § 2143.01, "[i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)."[2] Clark is clear that the heavy doping for the guard ring (220) must be concentrated at the surface of the substrate (204) to avoid extending to the lower areas of the STI (202/205), especially the bottom parts (218) thereof, which may cause, not reduce dark current according to Clark. Clark col. 3, l. 50 to col. 4, l. 20. Limiting the interaction of the dopant guard ring (220) and the STI (202) to a lateral surface (228) of the STI (202) is key to improving

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[2] In the same section, the M.P.E.P further states:

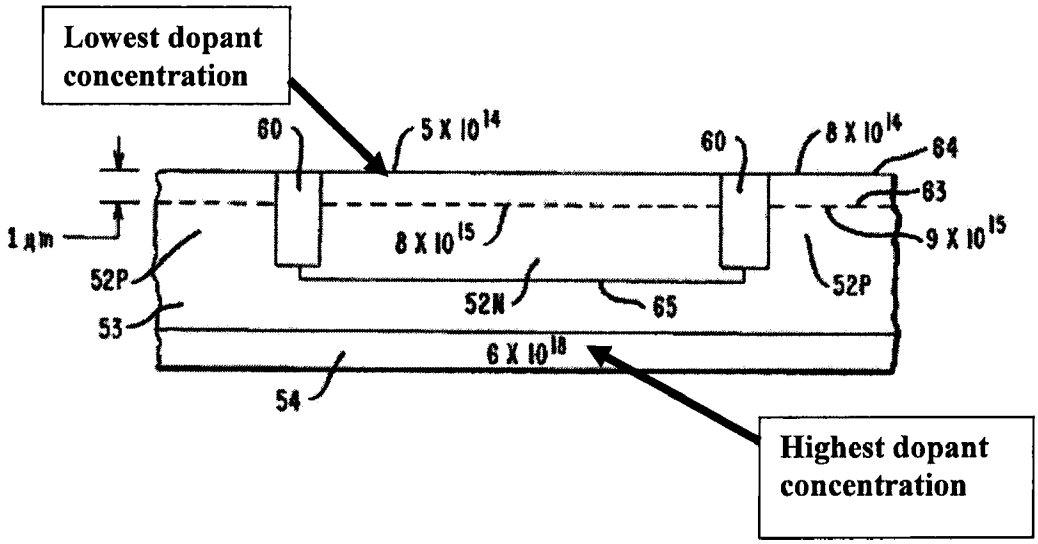
> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) . . . . [T]he "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." 270 F.2d at 813, 123 USPQ at 352.).

Here, too, Clark would have to be substantially reconstructed to make the combination with Mundt and, thus, this combination is improper as a matter of law.

the current leakage problems identified by Clark – the dopant area must not extend below the STI (202). Clark col. 3, ll. 59-62; col. 4, ll. 13-20.

Mundt, discloses "retrograde" dopant profiles such that the dopant concentration must be lower toward the substrate surface and higher in a direction away from the substrate surface (Mundt col. 1, ll. 7-15). Even the portion of Mundt specifically cited by the Final Rejection (at 5) is clear on this: "In accordance with the present invention, an indiffusion-outdiffusion process is used to form the n-well 52N and p-well 52P and to form a retrograde vertical dopant profile for such wells, in which profile the doping level at depth within the substrate, indicated by line 63 (FIG. 7), exceeds the doping level at the substrate surface." Mundt col. 5, ll. 27-33 (emphasis added). Mundt illustrates this at Fig. 7, which shows the dopant implant concentrations at various depths of the substrate; this figure is reproduced (and annotated) below:

FIG. 7



Changing the Clark dopant profile from that expressly taught by Clark (heavily doped substrate surface – Clark col. 3, ll. 31-33) to be just the opposite as disclosed by Mundt (lightly doped surface and heavily doped at depth – Mundt col. 5, ll. 30-31) would render Clark's essential guard ring (220) seemingly inoperable, and according to Clark would cause increased

problems (more dark current – Clark col. 4, ll. 4-6). It would extend the dopant to the bottom of the STI (202) at surface (218 – an interface between the STI and the underlying substrate), which would negate the charge leakage protection Clark indicates it provides.

It is clear that the doping profile of Mundt's retrograde well is incompatible with the structure of Clark as it is exactly the opposite from what Clark specifically requires in a doping profile. Incorporation of the Mundt well (52P) into the Clark device would make the device of Clark unsatisfactory for its intended purpose and seemingly inoperable. Therefore, Clark (requiring high dopant at the substrate surface) and Mundt (requiring high dopant at a substrate depth) each specifically teach away from their combination and their combination is improper as a matter of law.

Furthermore, even if the references did not teach away from their combination, which they do, or the Clark invention would function for its intended purpose with the Mundt well, which it would not according to the disclosure of Clark, or if either reference expressly recognized the problem of charge loss from an imager array, which they do not, there still would be no motivation to combine the retrograde well of Mundt with the photosensor device of Clark because the device of Clark already deals with charge leakage in its own way. As identified above, the present application explains that the primary advantages associated with including the recited "retrograde well being doped with a vertically graded dopant profile" (the feature identified in the Final Rejection as missing in Clark and supplied by Mundt) with imager pixels as being the prevention of loss of signal from and intrusion of unwanted signals into the pixel – each associated with signal leakage. Leakage prevention between pixels is indicated by Clark to be provided by its Heavily Doped Region guard ring (220). Clark col. 1, ll. 27-43; col. 4, ll. 4-20. Therefore, there is no reason, suggestion, or motivation to add yet another feature to the Clark device such as a retrograde well as recited in claim 70 to ostensibly achieve the same or similar leakage mitigation.

4. The Final Rejection Fails To Establish A *Prima Facie* Case For Obviousness

Furthermore, the Final Rejection fails to make a proper *prima facie* case for obviousness. As explained at M.P.E.P. § 2141:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR* noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Court quoting *In re Kahn,* 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), stated that "'[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.'" *KSR*, 550 U.S. at ___, 82 USPQ2d at 1396.

Here, there is no clear articulation of any reason why the claimed subject matter is obvious, other than the conclusory statements that all the limitations can be found in the prior art. This, without more, is not enough to satisfy the Supreme Court. Furthermore, the M.P.E.P. § 2143.01 states:

> A statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). "'[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.'" *KSR*, 550 U.S. at ___, 82 USPQ2d at 1396 quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

The Board recently ruled on similar facts in *Ex parte Chandler*, 2008 WL 2233745, Appeal 2007-3120 (Bd. Pat. App. & Interf. May 30, 2008), that the examiner did not establish a *prima facie* case of obviousness on a proposed combination of references because the very feature lacking in the primary reference (using fluorescent classification to distinguish particles),

for which a combination was required, was explicitly avoided by the primary reference. For this reason, the examiner could not establish a good reason the references should be combined or the motivation to do so. *Id.* The present case is analogous because, as discussed above, the primary reference requires the opposite dopant profile as the secondary reference, thus, Clark avoids the specific teaching for which Mundt is cited and they cannot be combined as a matter of law.

Without improperly applying hindsight reasoning with the present application as a roadmap, the Final Rejection's reasoning allegedly identifying a motivation to combine Clark and Mundt is incorrect. *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351 (Fed. Cir. 2001) (claimed invention was a baseball with finger position marks – held not obvious). The Federal Circuit notes that, as a useful general rule, references that teach away cannot serve to create a *prima facie* case of obviousness. *Id.* at 1353-54. If references taken in combination would produce a seemingly inoperative device, then they teach away from the combination and cannot serve as predicates for a *prima facie* case of obviousness. *Id.* at 1354. As discussed above, the references clearly teach away from their combination since reversing Clark's doping profile to that of Mundt would make Clark's device seemingly inoperable according to Clark.

For the above reasons, e.g., the cited art does not teach every claim element and is improperly combined as a matter of law, independent claim 70 is patentable over Clark and Mundt. Likewise, each dependent claim, 71-79, is also patentable over these references. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 70 be reversed and withdrawn and the rejected claims allowed.

5. Independent Claim 120 Is Patentable For At Least The Same Reasons Set Forth Above In Relation To The Patentability of Independent Claim 70.

Claim 120 defines a CMOS imager and recites "an array of pixel sensor cells formed in a retrograde well in a substrate, the retrograde well being doped with a vertically graded dopant concentration, wherein each of said pixel sensor cells is separated by an isolation region that electrically isolates said pixel cells from each other, and each said pixel sensor cell

comprises: a photoconversion device; a reset transistor; a source follower transistor; a row select transistor; and a floating diffusion region in electrical communication with said photoconversion device and said source follower transistor." Such a device not would not have been obvious over Clark and Mundt.

Similar to independent claim 70, independent claim 120 recites "an array of pixel sensor cells formed in a retrograde well being doped with a vertically graded dopant concentration." As with the rejection of claim 70, the Final Rejection (at 5) relies on the teachings of Mundt to be combined with Clark to provide such a feature. However, as discussed above, Clark and Mundt fail to teach the application of a retraograde well to an array of anything, much less of pixel sensor cells, and the references are not properly combinable for this (or any other relevant) purpose. The references are incompatible and teach away from their combination and combining the references would prevent the device of Clark from performing its intended purpose. Also, there is simply no logical reason to add the features of Mundt to Clark, in part, because the Clark structure already achieves the same or similar advantages that the Mundt features would allegedly provide. Finally, the Final Rejection fails to establish a *prima facie* case for combining Clark and Mundt or for the obviousness of the claimed subject matter.

For the above reasons, independent claim 120 is patentable over the Clark and Mundt combination. Likewise, each dependent claim, 121-130, is also patentable over these references. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 120 and 122-124 be reversed and withdrawn and the rejected claims allowed.

D. Claims 71-79 and 125-130 are patentable under 35 U.S.C. § 103(a) over Clark in view of Mundt and further in view of Burr. These claims are dependent from patentable claims and Burr adds nothing to overcome the deficiencies of the Clark-Mundt combination.

Claims 71-79 depend from independent claim 70 and claims 125-130 depend from independent claim 120, each of which is patentable over the Clark and Mundt combination, as

discussed above. Burr is cited in the Final Rejection (at 7-10) for its alleged disclosure of an array of pixel sensor cells and a processor being formed on a single substrate. Even if Burr contained such a disclosure, which it does not, the combination of Burr and either of Clark or Mundt (which cannot be combined, themselves) would not satisfy each and every limitation of independent claims 70 and 120. Burr does not teach or suggest an array of pixel sensor cells, it is directed to MOS (metal-oxide-semiconductor) transistors, like Mundt. The Final Rejection even notes this (at 7). Like Mundt, Burr would not have been combined with Clark to achieve or render obvious the claimed invention.

For the above reasons, claims 71-79 and 125-130 are patentable over the Clark, Mundt, and Burr combination. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of these claims be reversed and withdrawn and the claims allowed.

E. Claim 121 is patentable under 35 U.S.C. § 103(a) over Clark in view of Mundt and further in view of Guidash. This claim is dependent from a patentable claim and Guidash adds nothing to overcome the deficiencies of the Clark-Mundt combination.

Claim 121 depends from independent claim 120, which is patentable over the Clark and Mundt combination, as discussed above. Guidash is cited in the Final Rejection (at 11) for its alleged disclosure of a transfer transistor positioned to gate charges between a photoconversion device and a floating diffusion region. Even if Guidash contained such a disclosure, the combination of Guidsh and either of Clark or Mundt (again, not combinable themselves) would not satisfy each and every limitation of independent claim 120. Such a combination would still lack the retrograde well features of the claim.

For the above reasons, claim 121 is patentable over Clark, Mundt, and Guidash. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of this claim be reversed and withdrawn and the claim allowed.

F. Conclusion

In view of the above, Applicants believe the pending application is in condition for allowance. Applicants respectfully request that the outstanding rejection of the claims be REVERSED by the Board and withdrawn by the Examiner and that a Notice of Allowance be immediately mailed.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: January 15, 2009

Respectfully submitted,

By_____

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Attachments:

Claims Appendix A
Evidence Appendix B
Related Proceedings Appendix C
U.S. Patent Application Pub. No. 2004/0150736 Appendix D

APPENDIX A

The following is a listing of the Claims Involved in the Appeal of Application Serial No. 10/761,319:

1-69. (Canceled).

70. (Previously Presented) An imager comprising:

an array of pixel sensor cells formed in a retrograde well on a substrate, the retrograde well being doped with a vertically graded dopant profile, wherein each pixel sensor cell has a photosensitive region and a photosensor formed at the photosensitive region;

a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image; and

a processor for receiving and processing data representing the image.

71. (Previously Presented) The imager of claim 70, wherein said array of pixel sensor cells and said processor are formed on a single substrate.

72. (Previously Presented) The imager of claim 70, wherein said array of pixel sensor cells is formed on a first substrate, and said processor is formed on a second substrate.

73. (Previously Presented) The imager of claim 70, wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of the retrograde well.

74. (Previously Presented) The imager of claim 73, wherein the retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well.

75. (Previously Presented) The imager of claim 70, wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of the retrograde well.

76. (Previously Presented) The imager of claim 75, wherein the retrograde well has a dopant concentration within the range of about 1 x 10^{15} to 5 x 10^{16} atoms per cm^3 at the top of the retrograde well.

77. (Previously Presented) The imager of claim 70, wherein the retrograde well has a dopant concentration of about 3 x 10^{17} atoms per cm^3 at the bottom of the retrograde well.

78. (Previously Presented) The imager of claim 77, wherein the retrograde well has a dopant concentration of about 5 x 10^{15} atoms per cm^3 at the top of the retrograde well.

79. (Previously Presented) The imager of claim 70, wherein the retrograde well is a first retrograde well, and said circuit is formed in a second retrograde well.

80-119. (Canceled).

120. (Previously Presented) A CMOS imager comprising:

an array of pixel sensor cells formed in a retrograde well in a substrate, the retrograde well being doped with a vertically graded dopant concentration, wherein each of said pixel sensor cells is separated by an isolation region that electrically isolates said pixel cells from each other, and each said pixel sensor cell comprises:

a photoconversion device;

a reset transistor;

a source follower transistor;

a row select transistor; and

a floating diffusion region in electrical communication with said photoconversion device and said source follower transistor.

121. (Previously Presented) The CMOS imager of claim 120 wherein the photoconversion device further comprises a transfer transistor positioned to gate charges between said photoconversion device to said floating diffusion region.

122. (Previously Presented) The CMOS imager of claim 120 wherein the photoconversion device is a photogate.

123. (Previously Presented) The CMOS imager of claim 120 wherein the photoconversion device is a photodiode.

124. (Previously Presented) The CMOS imager of claim 120 wherein the photoconversion device is a photoconductor.

125. (Previously Presented) The CMOS imager of claim 120 wherein said retrograde well is provided to reflect signal carriers back to the photoconversion device.

126. (Previously Presented) The CMOS imager of claim 120 wherein said vertically graded dopant concentration of the retrograde well is highest at a top of the well and lowest at a bottom of the well.

127. (Previously Presented) The CMOS imager of claim 120, wherein said vertically graded dopant concentration of the retrograde well is lowest at a top of the well and highest at a bottom of the well.

128. (Previously Presented) The CMOS imager of claim 127, wherein said vertically graded dopant concentration at the top of the retrograde well is within the range of about 5×10^{14} to 1×10^{17} atoms per cm^3 and the concentration at the bottom of the retrograde well is within the range of about 1×10^{16} to 2×10^{18} atoms per cm^3.

129. (Previously Presented) The CMOS imager of claim 127, wherein said vertically graded dopant concentration at the top of the retrograde well is within the range of about 1×10^{15} to 5×10^{16} atoms per cm^3 and the concentration at the bottom of the retrograde well is within the range of about 5×10^{16} to 1×10^{18} atoms per cm^3.

130. (Previously Presented) The CMOS imager of claim 127, wherein said vertically graded dopant concentration at the top of the retrograde well is about 5×10^{15} atoms per cm^3 and the concentration at the bottom of the retrograde well is about 3×10^{17} atoms per cm^3.

APPENDIX B

No evidence pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

A copy of the Terminal Disclaimer filed January 12, 2009, discussed above, is attached hereto.

Technical evidence regarding the condition of "latchup" in circuits is attached.

PTO/SB/26 (11-08)
Approved for use through 12/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) M4065.0107/P107-F

In re Application of: Howard E. Rhodes et al.

Application No.: 10/761,319-Conf. #2671

Filed: January 22, 2004

For: TWIN PWELL WITH A RETROGRADE PWELL FOR CMOS IMAGERS

The owner*, Aptina Imaging Corporation, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 6,310,336 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 28,371

Signature — January 12, 2009 (Date)

Thomas J. D'Amico
Typed or printed name

(202) 420-2232
Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Docket No.: M4065.0107/P107-F
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Howard E. Rhodes et al.

Application No.: 10/761,319 Confirmation No.: 2671

Filed: January 22, 2004 Art Unit: 2622

For: RETROGRADE WELL STRUCTURE FOR A CMOS IMAGER Examiner: Chia W. A. Chen

REMARKS ACCOMPANYING TERMINAL DISCLAIMER

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REMARKS

Claims 70-79 stand rejected on the ground of nonstatutory obviousness-type double patenting over claims 36-45 of U.S. Patent No. 6,310,366 ("Rhodes et al."). Claims 120-130 stand rejected on the ground of nonstatutory obviousness-type double patenting over claims 20-35 of Rhodes et al. in view of U.S. Patent 5,471,515 ("Fossum"). In view of the terminal disclaimer to Rhodes et al. submitted herewith, the rejections should be withdrawn.

Dated: January 12, 2009

Respectfully submitted,

By _____
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Attorneys for Applicants

Latchup

From Wikipedia, the free encyclopedia

Latchup is a term used in the realm of integrated circuits (*microchips*) to describe a particular type of short circuit which can occur in an improperly designed circuit. More specifically it is the inadvertent creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disrupts proper functioning of the part and possibly even leading to its destruction due to overcurrent. A power cycle is required to correct this situation.

The parasitic structure is usually equivalent to a thyristor (or SCR), a PNPN structure which acts as a PNP and an NPN transistor stacked next to each other. During a latchup when one of the transistors is conducting, the other one begins conducting too. They both keep each other in saturation for as long as the structure is forward-biased and some current flows through it - which usually means until a power-down. The SCR parasitic structure is formed as a part of the totem-pole PMOS and NMOS transistor pair on the output drivers of the gates.

The latchup does not have to happen between the power rails; it can happen at any place where the required parasitic structure exists. A spike of positive or negative voltage on an input or output pin of a digital chip, exceeding the rail voltage by more than a diode drop, is a common cause of latchup. Another cause is the supply voltage exceeding the absolute maximum rating, often from a transient spike in the power supply, leading to a breakdown of some internal junction. This frequently happens in circuits which use multiple supply voltages that do not come up in the proper order after a power-up, leading to voltages on data lines exceeding the input rating of parts that have not yet reached a nominal supply voltage.

Yet another common cause of latchups is ionizing radiation.

It is possible to design chips that are latchup-resistant, where a layer of insulating oxide (called a *trench*) surrounds both the NMOS and the PMOS transistors. This breaks the parasitic SCR structure between these transistors. Such parts are important in the cases where the proper sequencing of power and signals cannot be guaranteed (e.g., in hot swap devices). Most silicon-on-insulator devices are inherently latchup-resistant.

Another possibility for a latchup prevention is the *Latchup Protection Technology* circuit. When a latchup is detected, the LPT circuit shuts down the chip and holds it powered-down for a preset time.

Testing for Latchup

- See EIA/JEDEC STANDARD **IC Latch-Up Test** EIA/JESD78.
  This standard is commonly referenced in IC qualification specifications.

See also

- Electrostatic discharge: For qualification testing of semiconductor devices, ESD and latchup are commonly considered together.

External links

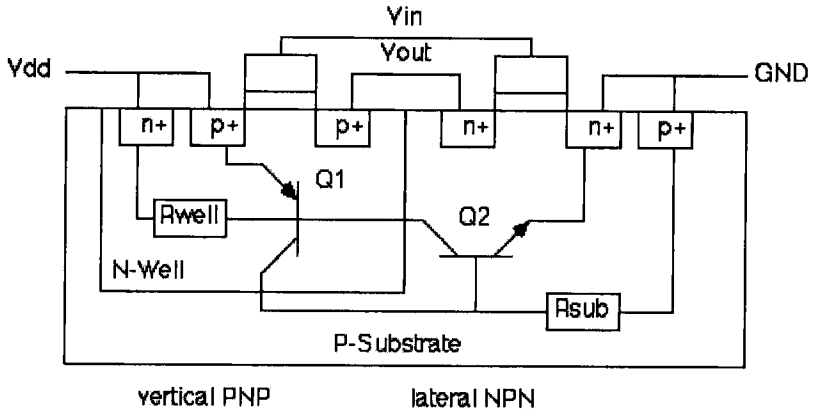
- Latch-up in CMOS designs (http://www.ece.drexel.edu/courses/ECE-E431/latch-up/latch-up.html)
- Analog Devices: Winning the battle against latchup in CMOS analog devices (http://www.analog.com/library/analogDialogue/archives/35-05/latchup/)
- Single-event latchup protection of integrated circuits (http://www.nasatech.com/Briefs/July98/0798ETB2.html)
- Maxwell Technologies Microelectronics: Latchup Protection Technology (http://www.maxwell.com/microelectronics/products/technologies/lpt_overview.html)
- Latch Up Overview (http://www.whitemountainlabs.com/latchup.aspx)

Retrieved from "http://en.wikipedia.org/wiki/Latchup"
Categories: Electronics terms | Integrated circuits

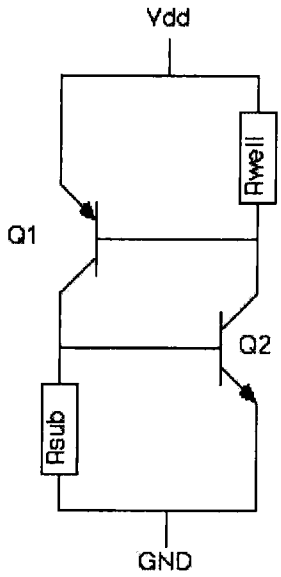
Microelectronics I Notes Supplement

Latchup in Bulk CMOS

A byproduct of the Bulk CMOS structure is a pair of parasitic bipolar transistors. The collector of each BJT is connected to the base of the other transistor in a positive feedback structure. A phenomenon called latchup can occur when (1) both BJT's conduct, creating a low resistance path between Vdd and GND **and** (2) the product of the gains of the two transistors in the feedback loop, b1 x b2, is greater than one. The result of latchup is at the minimum a circuit malfunction, and in the worst case, the destruction of the device.



Cross section of parasitic transistors in Bulk CMOS



Equivalent Circuit

Latchup may begin when Vout drops below GND due to a noise spike or an improper circuit hookup (Vout is the base of the lateral NPN Q2). If sufficient current flows through Rsub to turn on Q2 (I Rsub > 0.7 V), this will draw current through Rwell. If the voltage drop across Rwell is high enough, Q1 will also turn on, and a self-sustaining low resistance path between the power rails is formed. If the gains are such that b1 x b2 > 1, latchup may occur. Once latchup has begun, the only way to stop it is to reduce

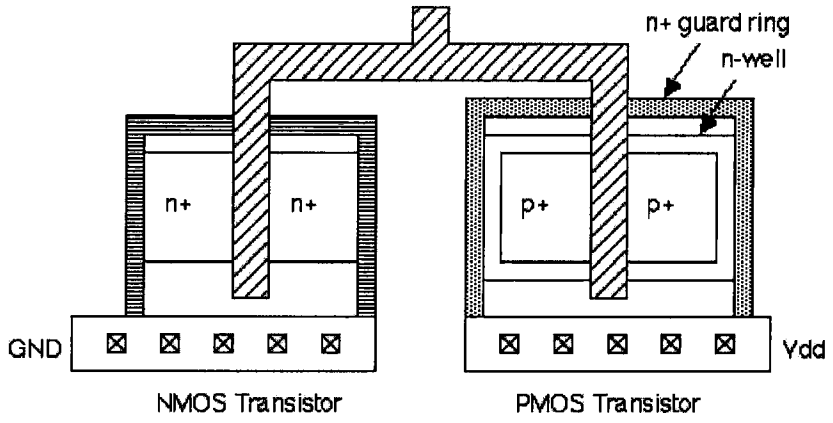
the current below a critical level, usually by removing power from the circuit.

The most likely place for latchup to occur is in pad drivers, where large voltage transients and large currents are present.

Preventing latchup

Fab/Design Approaches

1. Reduce the gain product b1 x b1
   - move n-well and n+ source/drain farther apart increases width of the base of Q2 and reduces gain beta2 > also reduces circuit density
   - buried n+ layer in well reduces gain of Q1
2. Reduce the well and substrate resistances, producing lower voltage drops
   - higher substrate doping level reduces Rsub
   - reduce Rwell by making low resistance contact to GND
   - guard rings around p- and/or n-well, with frequent contacts to the rings, reduces the parasitic resistances.



CMOS transistors with guard rings

Systems Approaches

1. Make sure power supplies are off before plugging a board. A "hot plug in" of an unpowered circuit board or module may cause signal pins to see surge voltages greater than 0.7 V higher than Vdd, which rises more slowly to is peak value. When the chip comes up to full power, sections of it could be latched.
2. Carefully protect electrostatic protection devices associated with I/O pads with guard rings. Electrostatic discharge can trigger latchup. ESD enters the circuit through an I/O pad, where it is clamped to one of the rails by the ESD protection circuit. Devices in the protection circuit can inject minority carriers in the substrate or well, potentially triggering latchup.
3. Radiation, including x-rays, cosmic, or alpha rays, can generate electron-hole pairs as they penetrate the chip. These carriers can contribute to well or substrate currents.
4. Sudden transients on the power or ground bus, which may occur if large numbers of transistors switch simultaneously, can drive the circuit into latchup. Whether this is possible should be checked through simulation.

APPENDIX C

No related proceedings are referenced in Part II above, hence copies of decisions in related proceedings are not provided.

APPENDIX D

A copy of U.S. Patent Application Pub. No. 2004/0150736 is attached. This is the published version of the present U.S. Patent Application Ser. No. 10/761,319.

US 20040150736A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2004/0150736 A1

Rhodes et al. (43) Pub. Date: Aug. 5, 2004

(54) RETROGRADE WELL STRUCTURE FOR A CMOS IMAGER

(76) Inventors: **Howard E. Rhodes**, Boise, ID (US); **Mark Durcan**, Boise, ID (US)

Correspondence Address:
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WASHINGTON, DC 20037-1526 (US)

(21) Appl. No.: **10/761,319**

(22) Filed: **Jan. 22, 2004**

Related U.S. Application Data

(60) Division of application No. 10/295,952, filed on Nov. 18, 2002, which is a continuation of application No. 09/918,450, filed on Aug. 1, 2001, now Pat. No. 6,483,129, which is a division of application No. 09/334,261, filed on Jun. 16, 1999, now Pat. No. 6,310,366.

Publication Classification

(51) **Int. Cl.**[7] **H04N 5/335**

(52) **U.S. Cl.** **348/308**

(57) ABSTRACT

A retrograde well structure for a CMOS imager that improves the quantum efficiency and signal-to-noise ratio of the imager. The retrograde well comprises a doped region with a vertically graded dopant concentration that is lowest at the substrate surface, and highest at the bottom of the well. A single retrograde well may have a single pixel sensor cell, multiple pixel sensor cells, or even an entire array of pixel sensor cells formed therein. The highly concentrated region at the bottom of the retrograde well repels signal carriers from the photosensor so that they are not lost to the substrate, and prevents noise carriers from the substrate from diffusing up into the photosensor. Also disclosed are methods for forming the retrograde well.

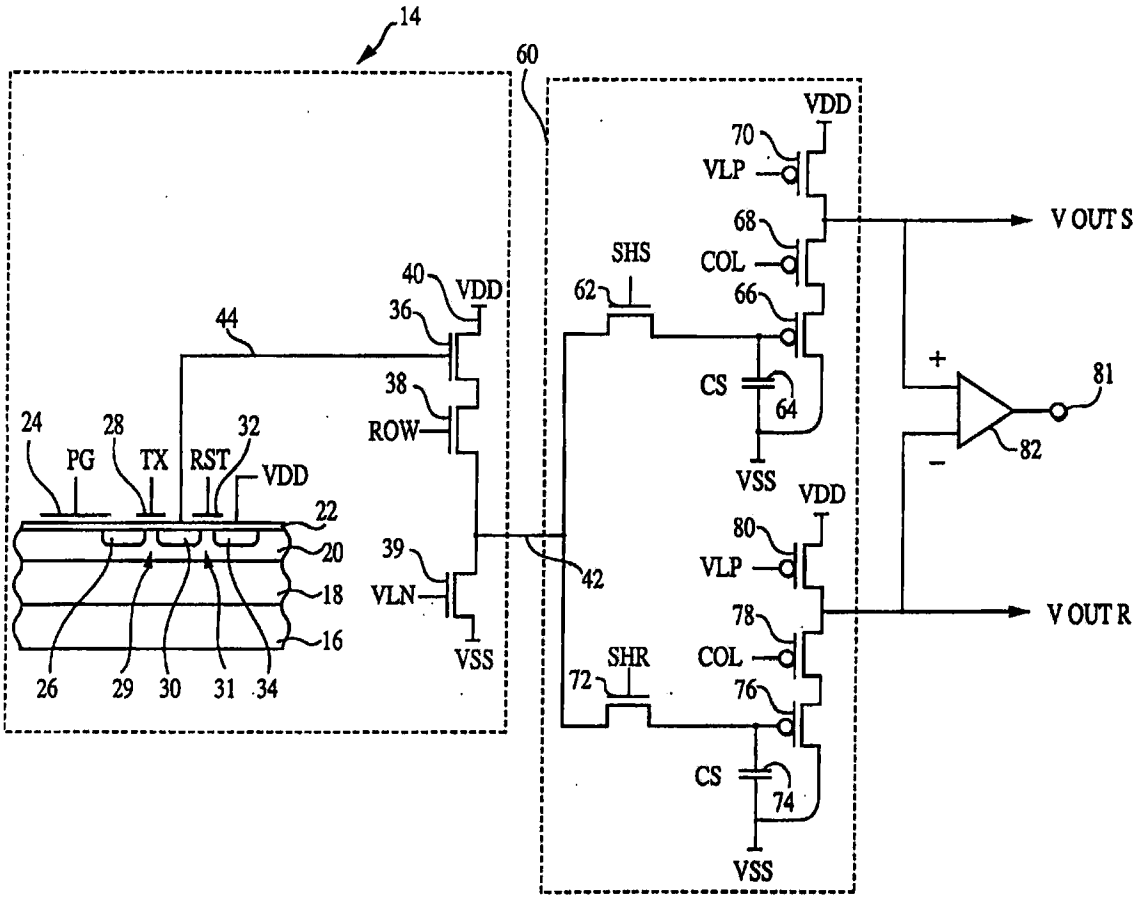


FIG. 1

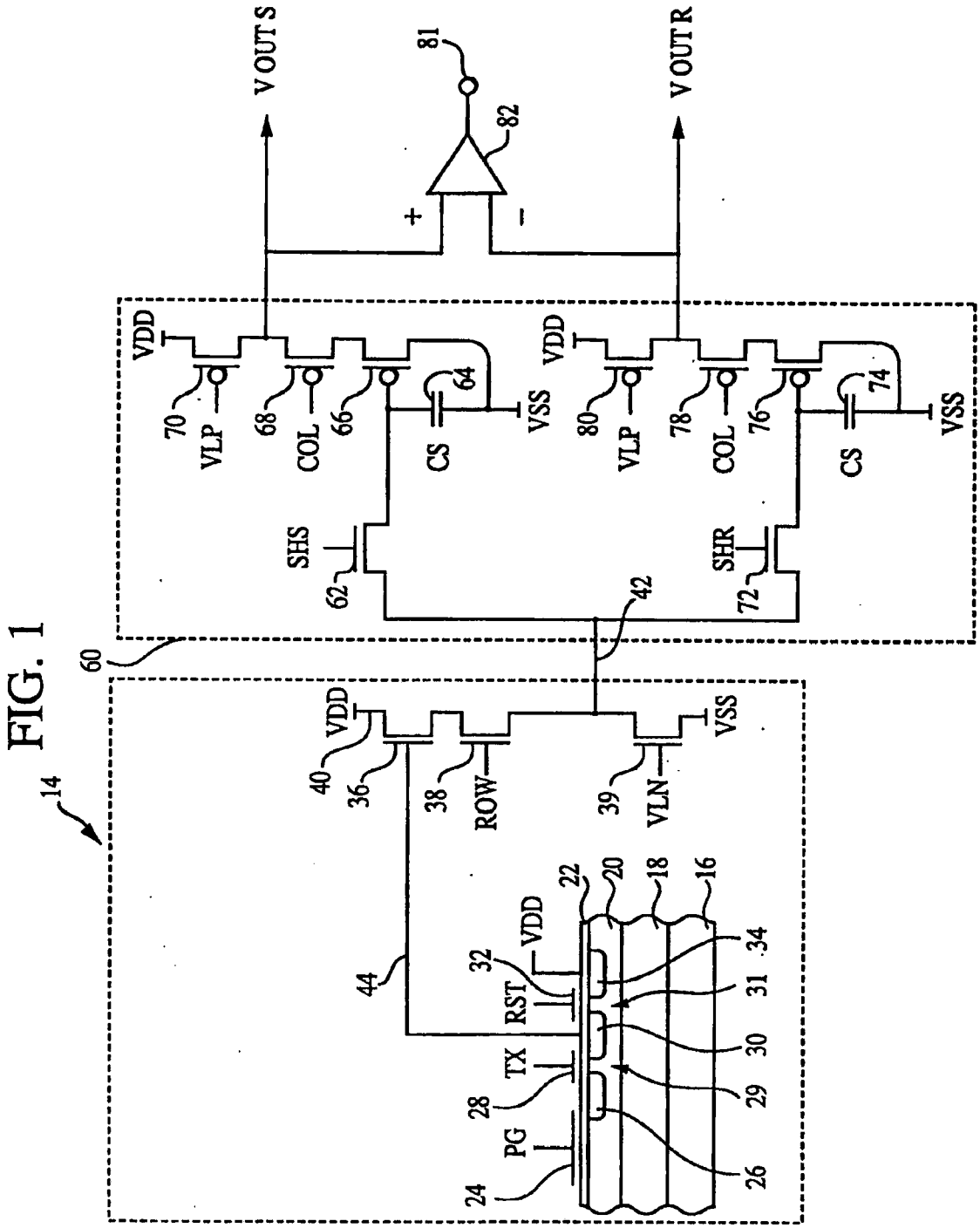

VOUTS
VOUTR
81
82
+
-
VDD
VDD
70
VLP
68
COL
66
64
CS
VSS
80
VLP
78
COL
76
74
CS
VSS
SHS
62
SHR
72
42
60
14
VDD
40
36
38
ROW
39
VLN
VSS
22
20
18
16
VDD
32
RST
34
31
44
TX
30
28
29
PG
24
26

FIG. 2

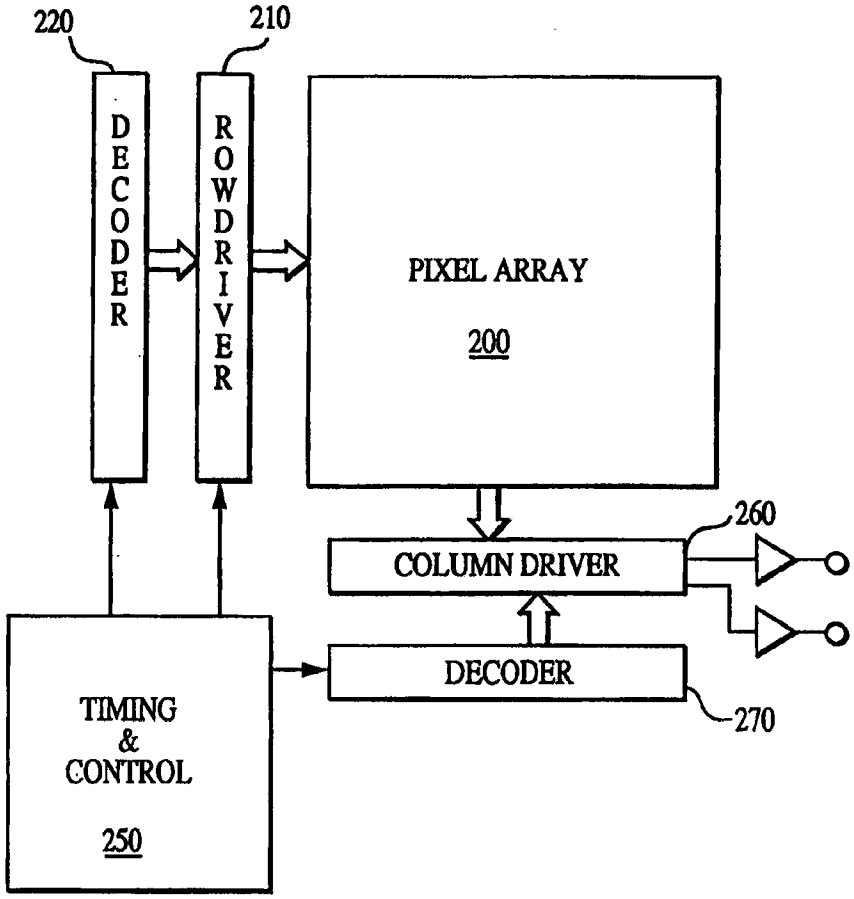

220
210
DECODER
ROWDRIVER
PIXEL ARRAY
200
260
COLUMN DRIVER
DECODER
270
TIMING
&
CONTROL
250

FIG. 3

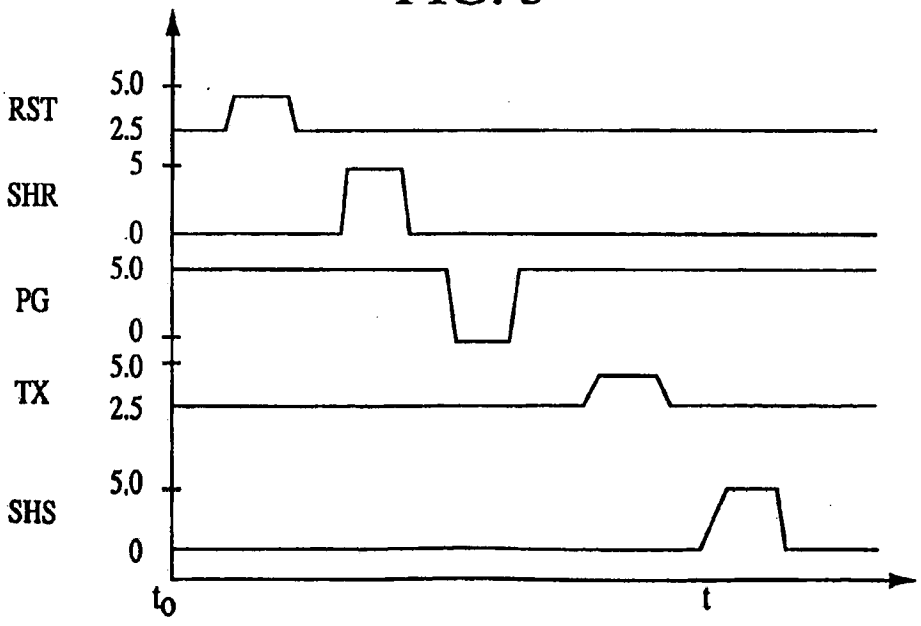
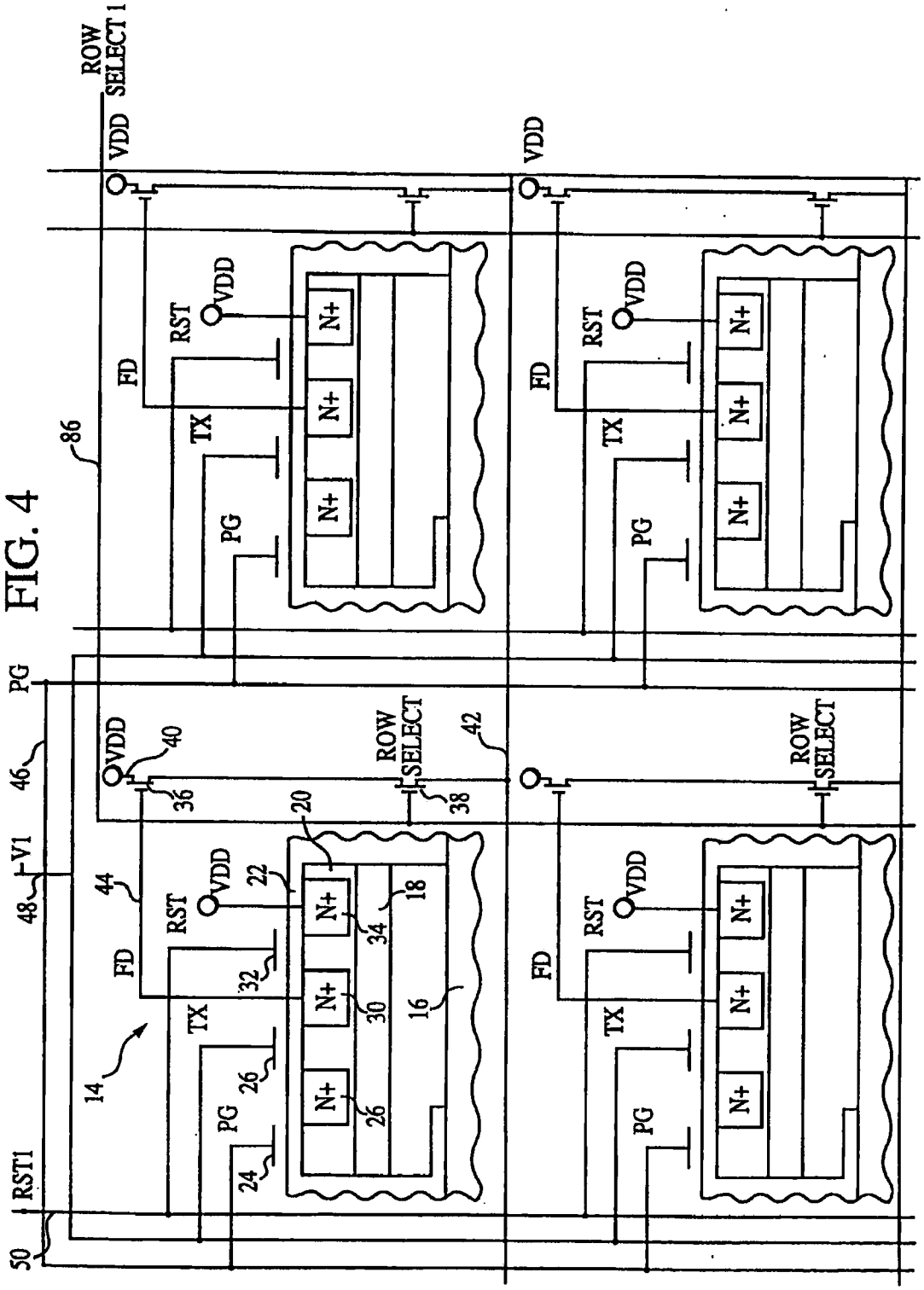

RST
SHR
PG
TX
SHS
5.0
2.5
5
0
5.0
0
5.0
2.5
5.0
0
t_0
t

FIG. 4


ROW SELECT 1
VDD
RST
FD
TX
PG
N+
86
46
V1
48
RST1
50
40
36
20
ROW SELECT
38
42
44
22
18
34
32
30
16
14
26
24

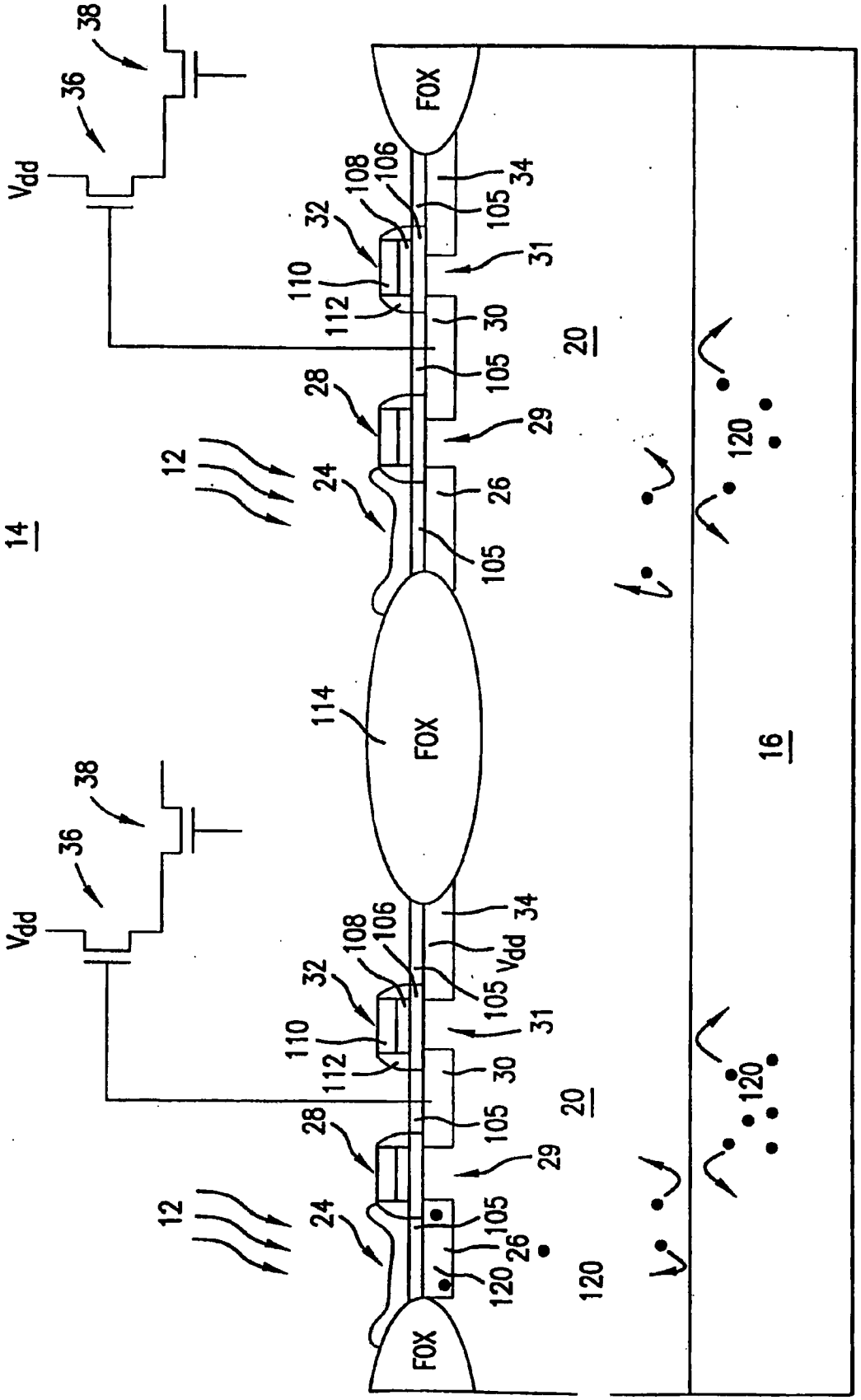

38
36
V_{dd}
FOX
108
106
34
105
32
31
110
112
30
20
28
29
12
24
26
14
114
16
120

FIG.5

FIG. 6

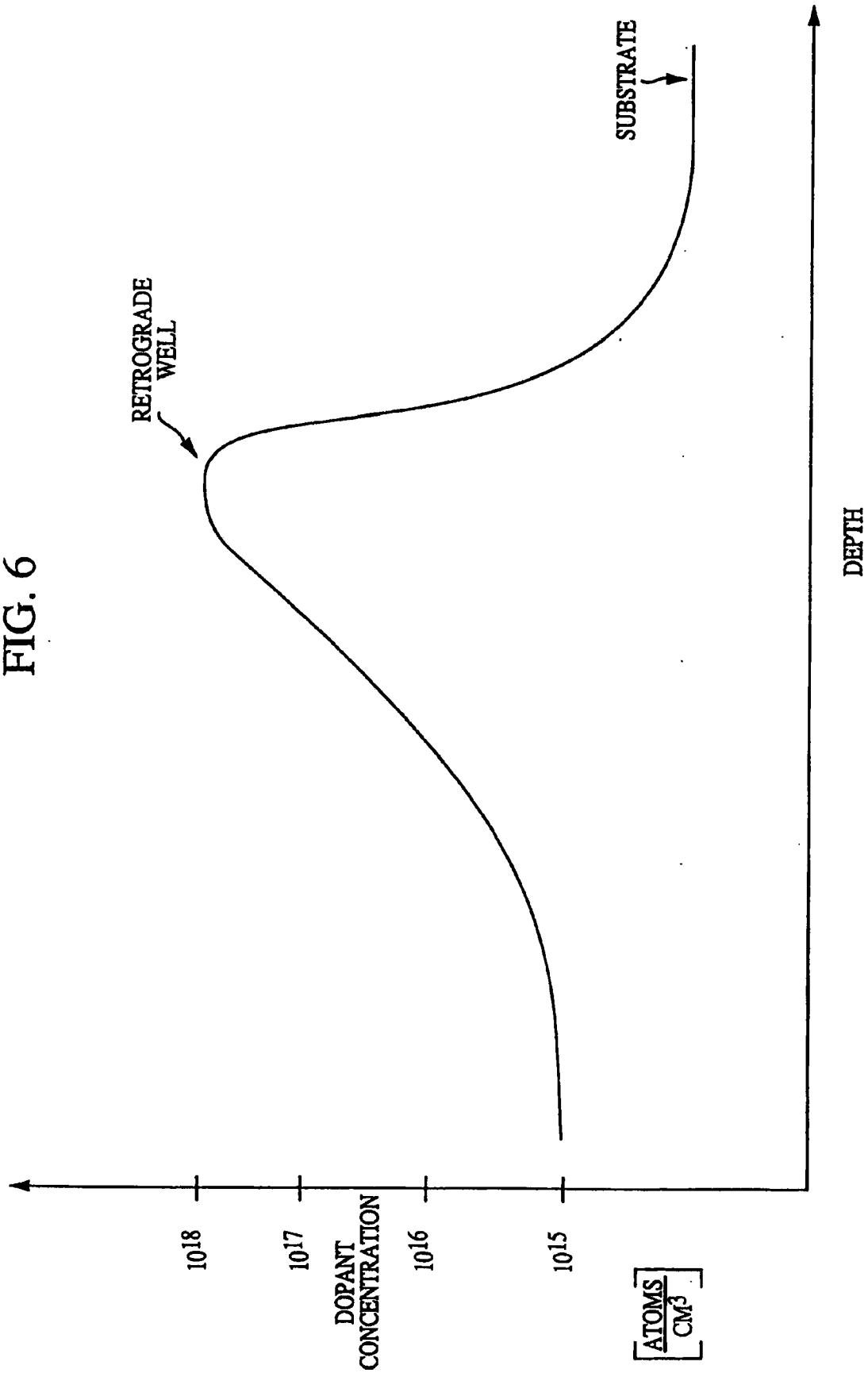

RETROGRADE WELL
SUBSTRATE
DEPTH
DOPANT CONCENTRATION
10^{18}
10^{17}
10^{16}
10^{15}
ATOMS / CM^3

FIG. 7

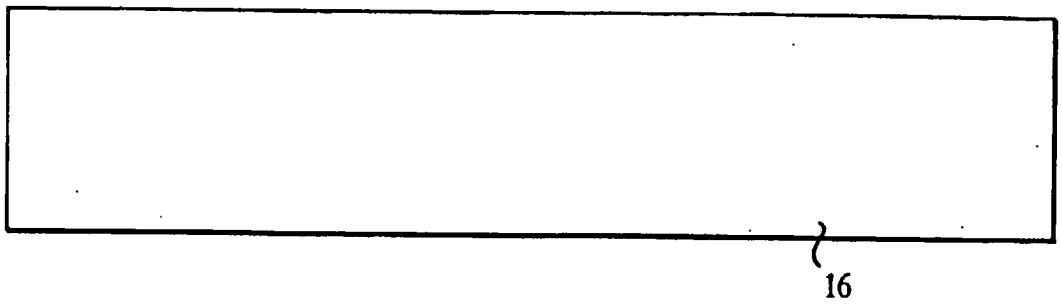


FIG. 8

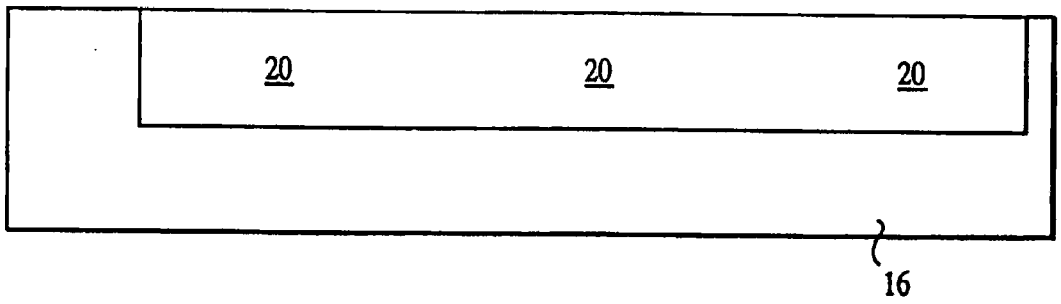


FIG. 9

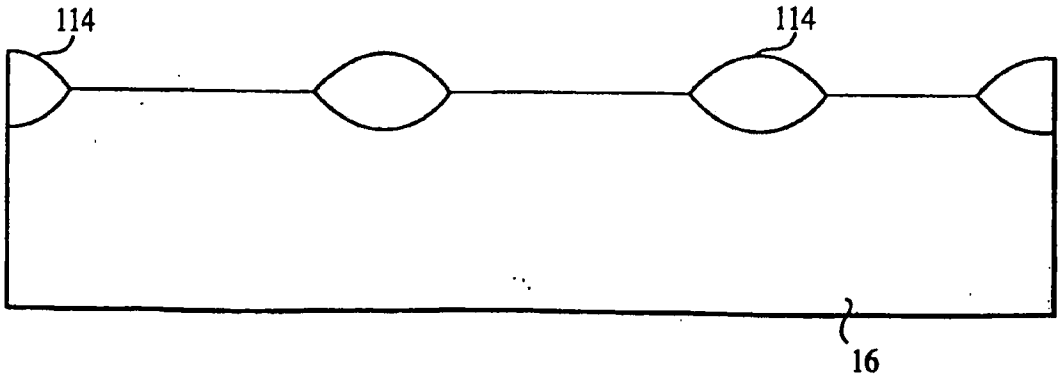


FIG. 10

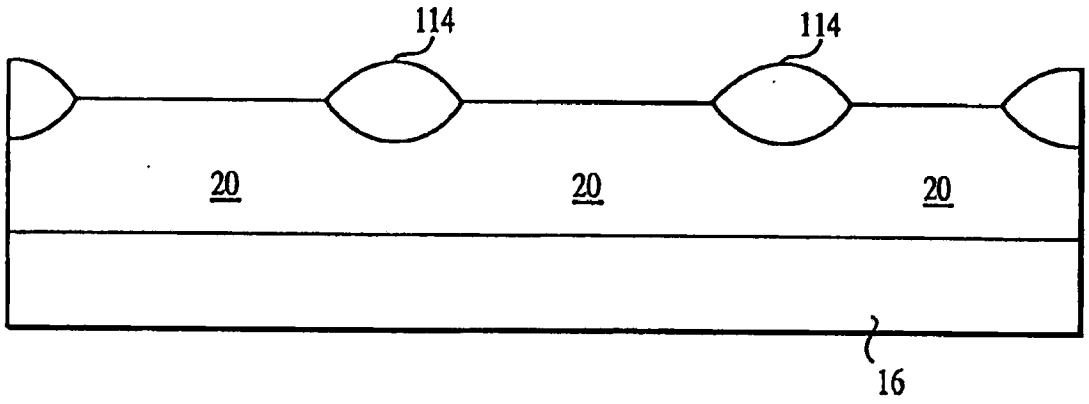
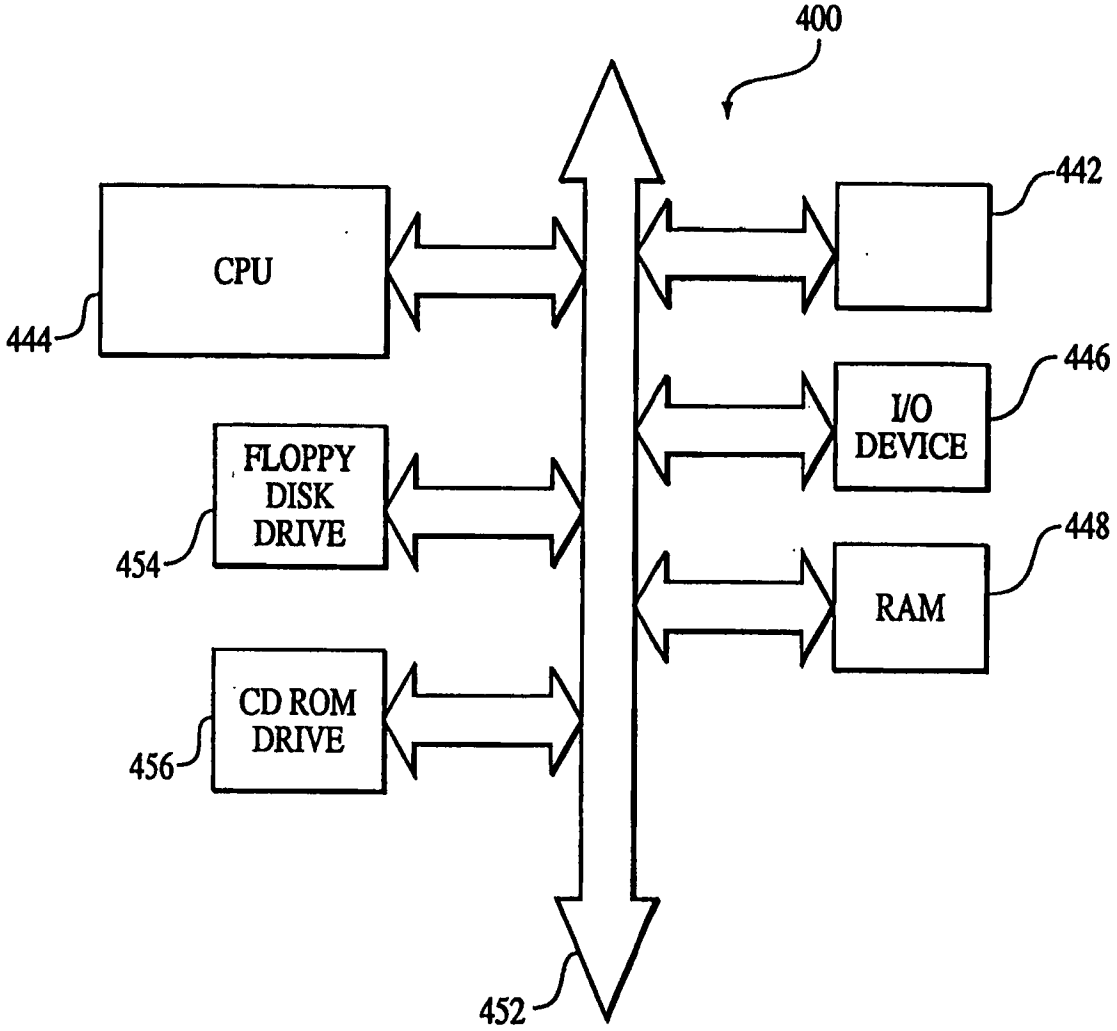


FIG. 11


400
442
CPU
444
I/O
DEVICE
446
FLOPPY
DISK
DRIVE
454
RAM
448
CD ROM
DRIVE
456
452

RETROGRADE WELL STRUCTURE FOR A CMOS IMAGER

FIELD OF THE INVENTION

[0001] The present invention relates generally to improved semiconductor imaging devices and in particular to a silicon imaging device that can be fabricated using a standard CMOS process.

BACKGROUND OF THE INVENTION

[0002] There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photodiode arrays, charge injection devices and hybrid focal plane arrays. CCD technology is often employed for image acquisition and enjoys a number of advantages which makes it the incumbent technology, particularly for small size imaging applications. CCDs are capable of large formats with small pixel size and they employ low noise charge domain processing techniques.

[0003] However, CCD imagers also suffer from a number of disadvantages. For example, they are susceptible to radiation damage, they exhibit destructive read-out over time, they require good light shielding to avoid image smear and they have a high power dissipation for large arrays. Additionally, while offering high performance, CCD arrays are difficult to integrate with CMOS processing in part due to a different processing technology and to their high capacitances, complicating the integration of on-chip drive and signal processing electronics with the CCD array. While there have been some attempts to integrate on-chip signal processing with CCD arrays, these attempts have not been entirely successful. CCDs also must transfer an image by line charge transfers from pixel to pixel, requiring that the entire array be read out into a memory before individual pixels or groups of pixels can be accessed and processed. This takes time. CCDs may also suffer from incomplete charge transfer from pixel to pixel which results in image smear.

[0004] Because of the inherent limitations in CCD technology, there is an interest in CMOS imagers for possible use as low cost imaging devices. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits would be beneficial to many digital applications such as, for example, in cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices, surveillance systems, auto focus systems, star trackers, motion detection systems, image stabilization systems and data compression systems for high-definition television.

[0005] The advantages of CMOS imagers over CCD imagers are that CMOS imagers have a low voltage operation and low power consumption; CMOS imagers are compatible with integrated on-chip electronics (control logic and timing, image processing, and signal conditioning such as A/D conversion); CMOS imagers allow random access to the image data; and CMOS imagers have lower fabrication costs as compared with the conventional CCD because standard CMOS processing techniques can be used. Additionally, low power consumption is achieved for CMOS imagers because only one row of pixels at a time needs to be active during the readout and there is no charge transfer (and associated switching) from pixel to pixel during image acquisition. On-chip integration of electronics is particularly advantageous because of the potential to perform many signal conditioning functions in the digital domain (versus analog signal processing) as well as to achieve a reduction in system size and cost.

[0006] A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photogate, photoconductor or a photodiode overlying a substrate for accumulating photo-generated charge in the underlying portion of the substrate. A readout circuit is connected to each pixel cell and includes at least an output field effect transistor formed in the substrate and a charge transfer section formed on the substrate adjacent the photogate, photoconductor or photodiode having a sensing node, typically a floating diffusion node, connected to the gate of an output transistor. The imager may include at least one electronic device such as a transistor for transferring charge from the underlying portion of the substrate to the floating diffusion node and one device, also typically a transistor, for resetting the node to a predetermined charge level prior to charge transference.

[0007] In a CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. Photo charge may be amplified when it moves from the initial charge accumulation region to the floating diffusion node. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate. For photodiodes, image lag can be eliminated by completely depleting the photodiode upon readout.

[0008] CMOS imagers of the type discussed above are generally known as discussed, for example, in Nixon et al., "256x256 CMOS Active Pixel Sensor Camera-on-a-Chip," IEEE Journal of Solid-State Circuits, Vol. 31(12), pp. 2046-2050 (1996); Mendis et al., "CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, Vol. 41(3), pp. 452-453 (1994), as well as U.S. Pat. No. 5,708,263 and U.S. Pat. No. 5,471,515, which are herein incorporated by reference.

[0009] To provide context for the invention, an exemplary CMOS imaging circuit is described below with reference to **FIG. 1**. The circuit described below, for example, includes a photogate for accumulating photo-generated charge in an underlying portion of the substrate. It should be understood that the CMOS imager may include a photodiode or other image to charge converting device, in lieu of a photogate, as the initial accumulator for photo-generated charge.

[0010] Reference is now made to **FIG. 1** which shows a simplified circuit for a pixel of an exemplary CMOS imager using a photogate and having a pixel photodetector circuit **14** and a readout circuit **60**. It should be understood that while **FIG. 1** shows the circuitry for operation of a single pixel, that in practical use there will be an MxN array of pixels arranged in rows and columns with the pixels of the

array accessed using row and column select circuitry, as described in more detail below.

[0011] The photodetector circuit **14** is shown in part as a cross-sectional view of a semiconductor substrate **16** typically a p-type silicon, having a surface well of p-type material **20**. An optional layer **18** of p-type material may be used if desired, but is not required. Substrate **16** may be formed of, for example, Si, SiGe, Ge, or GaAs. Typically the entire substrate **16** is p-type doped silicon substrate and may contain a surface p-well **20** (with layer **18** omitted), but many other options are possible, such as, for example p on p− substrates, p on p+ substrates, p-wells in n-type substrates or the like. The terms wafer or substrate used in the description includes any semiconductor-based structure having an exposed surface in which to form the circuit structure used in the invention. Wafer and substrate are to be understood as including silicon-on-insulator (SOI) technology, silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure or foundation.

[0012] An insulating layer **22** such as, for example, silicon dioxide is formed on the upper surface of p-well **20**. The p-type layer may be a p-well formed in substrate **16**. A photogate **24** thin enough to pass radiant energy or of a material which passes radiant energy is formed on the insulating layer **22**. The photogate **24** receives an applied control signal PG which causes the initial accumulation of pixel charges in n+ region **26**. The n+ type region **26**, adjacent one side of photogate **24**, is formed in the upper surface of p-well **20**. A transfer gate **28** is formed on insulating layer **22** between n+ type region **26** and a second n+ type region **30** formed in p-well **20**. The n+ regions **26** and **30** and transfer gate **28** form a charge transfer transistor **29** which is controlled by a transfer signal TX. The n+ region **30** is typically called a floating diffusion region. It is also a node for passing charge accumulated there at to the gate of a source follower transistor **36** described below.

[0013] A reset gate **32** is also formed on insulating layer **22** adjacent and between n+ type region **30** and another n+ region **34** which is also formed in p-well **20**. The reset gate **32** and n+ regions **30** and **34** form a reset transistor **31** which is controlled by a reset signal RST. The n+ type region **34** is coupled to voltage source V_{DD}, e.g., 5 volts. The transfer and reset transistors **29, 31** are n-channel transistors as described in this implementation of a CMOS imager circuit in a p-well. It should be understood that it is possible to implement a CMOS imager in an n-well in which case each of the transistors would be p-channel transistors. It should also be noted that while **FIG. 1** shows the use of a transfer gate **28** and associated transistor **29**, this structure provides advantages, but is not required.

[0014] Photodetector circuit **14** also includes two additional n-channel transistors, source follower transistor **36** and row select transistor **38**. Transistors **36, 38** are coupled in series, source to drain, with the source of transistor **36** also coupled over lead **40** to voltage source V_{DD} and the drain of transistor **38** coupled to a lead **42**. The drain of row select transistor **38** is connected via conductor **42** to the drains of similar row select transistors for other pixels in a given pixel row. A load transistor **39** is also coupled between the drain of transistor **38** and a voltage source V_{SS}, e.g. 0 volts. Transistor **39** is kept on by a signal V_{LN} applied to its gate.

[0015] The imager includes a readout circuit **60** which includes a signal sample and hold (S/H) circuit including a S/H n-channel field effect transistor **62** and a signal storage capacitor **64** connected to the source follower transistor **36** through row transistor **38**. The other side of the capacitor **64** is connected to a source voltage V_{SS}. The upper side of the capacitor **64** is also connected to the gate of a p-channel output transistor **66**. The drain of the output transistor **66** is connected through a column select transistor **68** to a signal sample output node V_{OUTS} and through a load transistor **70** to the voltage supply V_{DD}. A signal called "signal sample and hold" (SHS) briefly turns on the S/H transistor **62** after the charge accumulated beneath the photogate electrode **24** has been transferred to the floating diffusion node **30** and from there to the source follower transistor **36** and through row select transistor **38** to line **42**, so that the capacitor **64** stores a voltage representing the amount of charge previously accumulated beneath the photogate electrode **24**.

[0016] The readout circuit **60** also includes a reset sample and hold (S/H) circuit including a S/H transistor **72** and a signal storage capacitor **74** connected through the S/H transistor **72** and through the row select transistor **38** to the source of the source follower transistor **36**. The other side of the capacitor **74** is connected to the source voltage V_{SS}. The upper side of the capacitor **74** is also connected to the gate of a p-channel output transistor **76**. The drain of the output transistor **76** is connected through a p-channel column select transistor **78** to a reset sample output node V_{OUTR} and through a load transistor **80** to the supply voltage V_{DD}. A signal called "reset sample and hold" (SHR) briefly turns on the S/H transistor **72** immediately after the reset signal RST has caused reset transistor **31** to turn on and reset the potential of the floating diffusion node **30**, so that the capacitor **74** stores the voltage to which the floating diffusion node **30** has been reset.

[0017] The readout circuit **60** provides correlated sampling of the potential of the floating diffusion node **30**, first of the reset charge applied to node **30** by reset transistor **31** and then of the stored charge from the photogate **24**. The two samplings of the diffusion node **30** charges produce respective output voltages V_{OUTR} and V_{OUTS} of the readout circuit **60**. These voltages are then subtracted (V_{OUTS}–V_{OUTR}) by subtractor **82** to provide an output signal terminal **81** which is an image signal independent of pixel to pixel variations caused by fabrication variations in the reset voltage transistor **31** which might cause pixel to pixel variations in the output signal.

[0018] **FIG. 2** illustrates a block diagram for a CMOS imager having a pixel array **200** with each pixel cell being constructed in the manner shown by element **14** of **FIG. 1**. **FIG. 4** shows a 2×2 portion of pixel array **200**. Pixel array **200** comprises a plurality of pixels arranged in a predetermined number of columns and rows. The pixels of each row in array **200** are all turned on at the same time by a row select line, e.g., line **86**, and the pixels of each column are selectively output by a column select line, e.g., line **42**. A plurality of rows and column lines are provided for the entire array **200**. The row lines are selectively activated by the row

driver **210** in response to row address decoder **220** and the column select lines are selectively activated by the column driver **260** in response to column address decoder **270**. Thus, a row and column address is provided for each pixel. The CMOS imager is operated by the control circuit **250** which controls address decoders **220, 270** for selecting the appropriate row and column lines for pixel readout, and row and column driver circuitry **210, 260** which apply driving voltage to the drive transistors of the selected row and column lines.

[0019] **FIG. 3** shows a simplified timing diagram for the signals used to transfer charge out of photodetector circuit **14** of the **FIG. 1** CMOS imager. The photogate signal PG is nominally set to 5V and pulsed from 5V to 0V during integration. The reset signal RST is nominally set at 2.5V. As can be seen from the figure, the process is begun at time to by briefly pulsing reset voltage RST to 5V. The RST voltage, which is applied to the gate **32** of reset transistor **31**, causes transistor **31** to turn on and the floating diffusion node **30** to charge to the V_{DD} voltage present at n+ region **34** (less the voltage drop V_{TH} of transistor **31**). This resets the floating diffusion node **30** to a predetermined voltage (V_{DD}-V_{TH}). The charge on floating diffusion node **30** is applied to the gate of the source follower transistor **36** to control the current passing through transistor **38**, which has been turned on by a row select (ROW) signal, and load transistor **39**. This current is translated into a voltage on line **42** which is next sampled by providing a SHR signal to the S/H transistor **72** which charges capacitor **74** with the source follower transistor output voltage on line **42** representing the reset charge present at floating diffusion node **30**. The PG signal is next pulsed to **0** volts, causing charge to be collected in n+ region **26**.

[0020] A transfer gate voltage TX, similar to the reset pulse RST, is then applied to transfer gate **28** of transistor **29** to cause the charge in n+ region **26** to transfer to floating diffusion node **30**. It should be understood that for the case of a photogate, the transfer gate voltage TX may be pulsed or held to a fixed DC potential. For the implementation of a photodiode with a transfer gate, the transfer gate voltage TX must be pulsed. The new output voltage on line **42** generated by source follower transistor **36** current is then sampled onto capacitor **64** by enabling the sample and hold switch **62** by signal SHS. The column select signal is next applied to transistors **68** and **70** and the respective charges stored in capacitors **64** and **74** are subtracted in subtractor **82** to provide a pixel output signal at terminal **81**. It should also be noted that CMOS imagers may dispense with the transfer gate **28** and associated transistor **29**, or retain these structures while biasing the transfer transistor **29** to an always "on" state.

[0021] The operation of the charge collection of the CMOS imager is known in the art and is described in several publications such as Mendis et al., "Progress in CMOS Active Pixel Image Sensors," SPIE Vol. 2172, pp. 19-29 (1994); Mendis et al., "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," IEEE Journal of Solid State Circuits, Vol. 32(2) (1997); and Eric R Fossum, "CMOS Image Sensors: Electronic Camera on a Chip," IEDM Vol. 95, pp. 17-25 (1995) as well as other publications. These references are incorporated herein by reference.

[0022] Quantum efficiency is a problem in some imager applications due to the diffusion of signal carriers out of the photosite and into the substrate, where they become effectively lost. The loss of signal carriers results in decreased signal strength, increased cross talk, and the reading of an improper value for the adjacent pixels.

[0023] There is needed, therefore, an improved pixel sensor cell for use in an imager that exhibits improved quantum efficiency, a better signal-to-noise ratio, and reduced cross talk. A method of fabricating a pixel sensor cell exhibiting these improvements is also needed.

SUMMARY OF THE INVENTION

[0024] The present invention provides a pixel sensor cell formed in a retrograde well in a semiconductor substrate having improved quantum efficiency, an improved signal-to-noise ratio, and reduced cross talk. The retrograde well comprises a doped region with a vertically graded dopant concentration that is lowest at the substrate surface, and highest at the bottom of the well. The retrograde well would have an entire array of pixels formed therein, and may also have peripheral circuitry formed therein. If the peripheral circuitry is formed in the retrograde well, the well may have a different dopant profile in the peripheral region than in the array region. The highly concentrated region at the bottom of the retrograde well reflects signal carriers back to the photosensor so that they are not lost to the substrate. Also provided are methods for forming a pixel sensor cell in the retrograde well of the present invention.

[0025] Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] **FIG. 1** is a representative circuit of a CMOS imager.

[0027] **FIG. 2** is a block diagram of a CMOS pixel sensor chip.

[0028] **FIG. 3** is a representative timing diagram for the CMOS imager.

[0029] **FIG. 4** is a representative pixel layout showing a 2x2 pixel layout.

[0030] **FIG. 5** is a cross-sectional view of two pixel sensor cells according to an embodiment of the present invention.

[0031] **FIG. 6** is a graph depicting the dopant concentration as a function of the depth of the retrograde well.

[0032] **FIG. 7** is a cross-sectional view of a semiconductor wafer undergoing the process of a preferred embodiment of the invention.

[0033] **FIG. 8** shows the wafer of **FIG. 7** at a processing step subsequent to that shown in **FIG. 7**.

[0034] **FIG. 9** is a cross-sectional view of a semiconductor wafer undergoing the process of a second embodiment of the invention.

[0035] **FIG. 10** shows the wafer of **FIG. 9** at a processing step subsequent to that shown in **FIG. 9**.

[0036] **FIG. 11** is an illustration of a computer system having a CMOS imager according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0037] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

[0038] The terms "wafer" and "substrate" are to be understood as including silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, or gallium arsenide. For exemplary purposes an imager formed of n-channel devices in a retrograde p-well is illustrated and described, but it should be understood that the invention is not limited thereto, and may include other combinations such as an imager formed of p-channel devices in a retrograde n-well.

[0039] The term "pixel" refers to a picture element unit cell containing a photosensor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative pixel is illustrated in the figures and description herein, and typically fabrication of all pixels in an imager will proceed simultaneously in a similar fashion. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0040] The structure of pixel cells **14** formed in retrograde wells **20** of the first embodiment are shown in more detail in **FIG. 5**. A pixel cell **14** may be formed in a substrate **16** having a retrograde layer or well **20** of a first conductivity type, which for exemplary purposes is treated as p-type. The retrograde well **20** has a vertically graded dopant concentration that is lowest at the substrate surface, and highest at the bottom of the well, as is shown in **FIG. 6**. The dopant concentration at the top of the retrograde well **20** is within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3, and is preferably within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3, and most preferably is about 5×10^{15} atoms per cm^3. At the bottom of the retrograde well **20**, the dopant concentration is within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3, and is preferably within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3, and most preferably is about 3×10^{17} atoms per cm^3. A single retrograde well **20** as depicted in **FIG. 5**, spans all pixels in the array of pixels.

[0041] A second retrograde well (not shown) may be formed in the substrate **16**, and may have peripheral circuitry, such as, e.g., logic circuitry, formed therein. This second well may be doped similarly or differently from the first retrograde well **20**, for example, the first retrograde well **20** may be doped to a first dopant level such as about 3×10^{17} atoms per cm^3 at the bottom of the well and the second well may be doped to a second dopant level such as 5×10^{16} at the bottom of the well.

[0042] The transistor gates form the pixel cell **14** as shown: a photogate **24**, a transfer gate **28** for transfer transistor **29**, and a reset transistor gate **32** for the reset transistor **31**. In addition, the photosensitive element in the pixel cell **14** is shown to be a photogate **24**, but other photosensitive elements such as a photodiode or a photoconductor could be used. The source follower transistor and the row select transistor are not shown. The transfer gate **28** and the reset gate **32** include a gate oxide layer **106** on the retrograde well **20**, and a conductive layer **108** of doped polysilicon, tungsten, or other suitable material over the gate oxide layer **106**. An insulating cap layer **110** of, for example, silicon dioxide, silicon nitride, or ONO (oxide-nitride-oxide), may be formed if desired; also a more conductive layer such as a silicide layer (not shown) may be used between the conductive layer **108** and the cap **110** of the transfer gate stack **28**, source follower gate, row select gate, and reset gate stack **32**, if desired. Insulating sidewalls **112** are also formed on the sides of the gate stacks **28**, **32**. These sidewalls may be formed of, for example, silicon dioxide or silicon nitride or ONO. The transfer gate is not required but may advantageously be included. The photogate **24** is a semitransparent conductor and is shown as an overlapping gate. In this case there is a second gate oxide **105** over the retrograde well and under the photogate.

[0043] Underlying the photogate **24** is a doped region **26** called the photosite, where photogenerated charges are stored. In between the reset transistor gate **32** and the transfer gate **28** is a doped region **30** that is the source for the reset transistor **31**, and on the other side of the reset transistor gate **32** is a doped region **34** that acts as a drain for the reset transistor **31**. The doped regions **26**, **30**, **34** are doped to a second conductivity type, which for exemplary purposes is treated as n-type. The second doped region **30** is the floating diffusion region, sometimes also referred to as a floating diffusion node, and it serves as the source for the reset transistor **31**. The third doped region **34** is the drain of the reset transistor **31**, and is also connected to voltage source Vdd.

[0044] As shown in **FIG. 5**, as light radiation **12** in the form of photons strikes the photosite **26**, photo-energy is converted to electrical signals, i.e., carriers **120**, which are stored in the photosite **26**. The absorption of light creates electron-hole pairs. For the case of an n-doped photosite in a p-well, it is the electrons that are stored. For the case of a p-doped photosite in an n-well, it is the holes that are stored. In the exemplary pixel cell **14** having n-channel devices formed in a p-type retrograde well **20**, the carriers **120** stored in the photosite **26** are electrons. The retrograde well **20** acts to reduce carrier loss to the substrate **16** by forming a concentration gradient that modifies the band diagram and serves to reflect electrons back towards the photosite **26**, thereby increasing quantum efficiency of the pixel **14**.

[0045] The retrograde well **20** is manufactured through a process described as follows, and illustrated by **FIGS. 7 and 8**. Referring now to **FIG. 7, a** substrate **16**, which may be any of the types of substrates described above, is provided. Retrograde well **20** is then formed by suitable means such as

blanket ion implantation of the entire wafer. The retrograde well **20** may be implanted at a later stage of the process such as after field oxide formation. The implant may be patterned so that the array well and the periphery logic well could have different doping profiles.

[**0046**] Ion implantation is performed by placing the substrate **16** in an ion implanter, and implanting appropriate dopant ions into the substrate **16** at an energy of 100 keV to 5 MeV to form retrograde wells **20** having a dopant concentration that is lowest at the surface, and highest at the bottom of the well. The dopant concentration at the top of the retrograde well **20** is within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3, and is preferably within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3, and most preferably is about 5×10^{15} atoms per cm^3. At the bottom of the retrograde well **20**, the dopant concentration is within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3, and is preferably within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3, and most preferably is about 3×10^{17} atoms per cm^3. If the retrograde well is to be a p-type well, a p-type dopant, such as boron, is implanted, and if the well **20** is to be an n-type well, an n-type dopant, such as arsenic, antimony, or phosphorous is implanted. The resultant structure is shown in **FIG. 8**. Multiple high energy implants may be used to tailor the profile of the retrograde well **20**.

[**0047**] Referring now to **FIGS. 9 and 10**, field oxide regions **114** may be formed around the pixel cell **14** prior to the formation of the retrograde well **20**. The field oxide regions are formed by any known technique such as thermal oxidation of the underlying silicon in a LOCOS process or by etching trenches and filling them with oxide in an STI process. Following field oxide **114** formation, the retrograde wells **20** may then be formed by blanket implantation as shown in **FIG. 10** or by masked implantation (not shown).

[**0048**] Subsequent to formation of the retrograde well **20**, the devices of the pixel sensor cell **14**, including the photogate **24**, the transfer gate **28**, reset transistor **31**, the source follower **36** and the row select transistor **38** are formed by well-known methods. Doped regions **26**, **30**, and **34** are formed in the retrograde well **20**, and are doped to a second conductivity type, which for exemplary purposes will be considered to be n-type. The doping level of the doped regions **26**, **30**, **34** may vary but should be higher than the doping level at the top of the retrograde well **20**, and greater than 5×10^{16} atoms per cm^3. If desired, multiple masks and resists may be used to dope these regions to different levels. Doped region **26** may be variably doped, such as either n+ or n− for an n-channel device. Doped region **34** should be strongly doped, i.e., for an n-channel device, the doped region **34** will be doped as n+. Doped region **30** is typically strongly doped (n+), and would not be lightly doped (n−) unless a buried contact is also used.

[**0049**] The pixel sensor cell **14** is essentially complete at this stage, and conventional processing methods may be used to form contacts and wiring to connect gate lines and other connections in the pixel cell **14**. For example, the entire surface may then be covered with a passivation layer of, e.g., silicon dioxide, BSG, PSG, or BPSG, which is CMP planarized and etched to provide contact holes, which are then metallized to provide contacts to the photogate, reset gate, and transfer gate. Conventional multiple layers of conductors and insulators may also be used to interconnect the structures in the manner shown in **FIG. 1**.

[**0050**] A typical processor based system which includes a CMOS imager device according to the present invention is illustrated generally at **400** in **FIG. 11**. A processor based system is exemplary of a system having digital circuits which could include CMOS imager devices. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision system, vehicle navigation system, video telephone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

[**0051**] A processor system, such as a computer system, for example generally comprises a central processing unit (CPU) **444**, e.g., a microprocessor, that communicates with an input/output (I/O) device **446** over a bus **452**. The CMOS imager **442** also communicates with the system over bus **452**. The computer system **400** also includes random access memory (RAM) **448**, and, in the case of a computer system may include peripheral devices such as a floppy disk drive **454** and a compact disk (CD) ROM drive **456** which also communicate with CPU **444** over the bus **452**. CMOS imager **442** is preferably constructed as an integrated circuit which includes pixels containing a photosensor such as a photogate or photodiode formed in a retrograde well, as previously described with respect to **FIGS. 5 through 10**. The CMOS imager **442** may be combined with a processor, such as a CPU, digital signal processor or microprocessor, with or without memory storage in a single integrated circuit, or may be on a different chip than the processor.

[**0052**] As can be seen by the embodiments described herein, the present invention encompasses a pixel sensor cell formed in a retrograde well. The pixel sensor cell has improved quantum efficiency and an improved signal-to-noise ratio due to the presence of a doping gradient induced electric field created in the bottom of the retrograde well which reflects signal carriers back to the photosensitive node. By reflecting photogenerated carriers back to the storage node the retrograde p-well also reduces the number of carriers diffusing to adjacent pixels and so also reduces cross talk.

[**0053**] It should again be noted that although the invention has been described with specific reference to CMOS imaging circuits having a photogate and a floating diffusion region, the invention has broader applicability and may be used in any CMOS imaging apparatus. Similarly, the process described above is but one method of many that could be used. The above description and drawings illustrate preferred embodiments which achieve the objects, features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A pixel sensor cell for an imaging device, said pixel sensor cell comprising:

a retrograde well of a first conductivity type formed in a substrate;

a photosensitive region formed in said retrograde well; and

a floating diffusion region of a second conductivity type formed in said retrograde well for receiving charges transferred from said photosensitive region.

2. The pixel sensor cell of claim 1, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

3. The pixel sensor cell of claim 2, wherein said retrograde well is doped with boron.

4. The pixel sensor cell of claim 1, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

5. The pixel sensor cell of claim 4, wherein said retrograde well is doped with a dopant selected from the group consisting of arsenic, antimony, and phosphorous.

6. The pixel sensor cell of claim 1, wherein said retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of said retrograde well.

7. The pixel sensor cell of claim 6, wherein said retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of said retrograde well.

8. The pixel sensor cell of claim 1, wherein said retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of said retrograde well.

9. The pixel sensor cell of claim 8, wherein said retrograde well has a dopant concentration within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of said retrograde well.

10. The pixel sensor cell of claim 1, wherein said retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of said retrograde well.

11. The pixel sensor cell of claim 10, wherein said retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of said retrograde well.

12. The pixel sensor cell of claim 1, further comprising a photosensor formed on said photosensitive region for controlling the collection of charges in said photosensitive region.

13. The pixel sensor cell of claim 12, wherein said photosensor is a photodiode sensor.

14. The pixel sensor cell of claim 12, wherein said photosensor is a photogate sensor.

15. The pixel sensor cell of clam 12, wherein said photosensor is a photoconductor sensor.

16. The pixel sensor cell of claim 1, further comprising a transfer gate formed on said retrograde well between said photosensor and said floating diffusion region.

17. The pixel sensor cell of claim 1, further comprising a reset transistor formed in said retrograde well for periodically resetting a charge level of said floating diffusion region, said floating diffusion region being the source of said reset transistor.

18. The pixel sensor cell of claim 1, wherein said photosensitive region comprises a doped region of a second conductivity type.

19. A pixel sensor cell for an imaging device, said pixel sensor cell comprising:

a retrograde well of a first conductivity type formed in a substrate;

a photosensor formed in said retrograde well;

a reset transistor having a gate stack formed in said retrograde well;

a floating diffusion region of a second conductivity type formed in said retrograde well between said photosensor and reset transistor for receiving charges from said photosensor, said reset transistor operating to periodically reset a charge level of said floating diffusion region; and

an output transistor having a gate electrically connected to said floating diffusion region.

20. The pixel sensor cell of claim 19, wherein said photosensor further comprises a doped region of a second conductivity type located in said retrograde well.

21. The pixel sensor cell of claim 19, wherein said photosensor is a photodiode sensor.

22. The pixel sensor cell of claim 19, wherein said photosensor is a photoconductor sensor.

23. The pixel sensor cell of claim 19, further comprising a transfer gate located between said photosensor and said floating diffusion region.

24. The pixel sensor cell of claim 23, wherein said photosensor is a photogate sensor.

25. The pixel sensor cell of claim 19, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

26. The pixel sensor cell of claim 25, wherein said retrograde well is doped with boron.

27. The pixel sensor cell of claim 19, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

28. The pixel sensor cell of claim 27, wherein said retrograde well is doped with a dopant selected from the group consisting of arsenic, antimony, and phosphorous.

29. The pixel sensor cell of claim 19, wherein said retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of said retrograde well.

30. The pixel sensor cell of claim 29, wherein said retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of said retrograde well.

31. The pixel sensor cell of claim 19, wherein said retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of said retrograde well.

32. The pixel sensor cell of claim 31, wherein said retrograde well has a dopant concentration within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of said retrograde well.

33. The pixel sensor cell of claim 19, wherein said retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of said retrograde well.

34. The pixel sensor cell of claim 31, wherein said retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of said retrograde well.

35. A CMOS imager comprising:

a substrate having at least one retrograde well of a first conductivity type;

an array of pixel sensor cells formed in said at least one retrograde well, wherein each pixel sensor cell has a photosensor; and

a circuit electrically connected to receive and process output signals from said array.

36. The CMOS imager of claim 35, wherein said at least one retrograde well comprises one retrograde well.

37. The CMOS imager of claim 35, wherein said at least one retrograde well comprises a plurality of retrograde wells, wherein said array is formed in a first retrograde well of said plurality and said circuit is formed in a second retrograde well of said plurality.

38. The CMOS imager of claim 37, wherein said first retrograde well is doped to a first dopant level, and said second retrograde well is doped to a second dopant level.

39. The CMOS imager of claim 35, wherein each pixel sensor further comprises a floating diffusion region of a second conductivity type located in said at least one retrograde well.

40. The CMOS imager of claim 39, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

41. The CMOS imager of claim 40, wherein said at least one retrograde well is doped with boron.

42. The CMOS imager of claim 39, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

43. The CMOS imager of claim 42, wherein said at least one retrograde well is doped with a dopant selected from the group consisting of arsenic, antimony, and phosphorous.

44. The CMOS imager of claim 35, wherein each pixel sensor cell further comprises a transfer gate located between said photosensor and said floating diffusion region.

45. The CMOS imager of claim 44, wherein the photosensors are photogate sensors.

46. The CMOS imager of claim 35, wherein said at least one retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well.

47. The CMOS imager of claim 46, wherein said at least one retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of said at least one retrograde well.

48. The CMOS imager of claim 35, wherein said at least one retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well.

49. The CMOS imager of claim 48, wherein said at least one retrograde well has a dopant concentration within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of said at least one retrograde well.

50. The CMOS imager of claim 35, wherein said at least one retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of said at least one retrograde well.

51. The CMOS imager of claim 50, wherein said at least one retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of said at least one retrograde well.

52. The CMOS imager of claim 35, wherein the photosensors are photodiode sensors.

53. The CMOS imager of claim 35, wherein the photosensors are photoconductor sensors.

54. An imager comprising:

an array of pixel sensor cells formed in a substrate having at least one retrograde well of a first conductivity type, wherein each pixel sensor cell has a photosensor;

a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image; and

a processor for receiving and processing data representing the image.

55. The imager of claim 54, wherein said array, said circuit, and said processor are formed on a single substrate.

56. The imager of claim 54, wherein said array and said circuit are formed on a first substrate, and said processor is formed on a second substrate.

57. The imager of claim 54, wherein said at least one retrograde well comprises one retrograde well.

58. The imager of claim 54, wherein said at least one retrograde well comprises a plurality of retrograde wells, wherein said array is formed in a first retrograde well of said plurality and said circuit is formed in a second retrograde well of said plurality.

59. The imager of claim 57, wherein said first retrograde well is doped to a first dopant level, and said second retrograde well is doped to a second dopant level.

60. The imager of claim 54, wherein each pixel sensor cell further comprises a floating diffusion region of a second conductivity type located in said at least one retrograde well.

61. The imager of claim 60, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

62. The imager of claim 60, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

63. The imager of claim 54, wherein each pixel sensor cell further comprises a transfer gate located between said photosensor and said floating diffusion region.

64. The imager of claim 63, wherein the photosensors are photogate sensors.

65. The imager of claim 54, wherein said at least one retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well, and within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of said at least one retrograde well.

66. The imager of claim 54, wherein said at least one retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well, and within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of said at least one retrograde well.

67. The imager of claim 54, wherein said at least one retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of said at least one retrograde well, and about 5×10^{15} atoms per cm^3 at the top of said at least one retrograde well.

68. The imager of claim 54, wherein the photosensors are photodiode sensors.

69. The imager of claim 54, wherein the photosensors are photoconductor sensors.

70. An imager comprising:

a CMOS imager comprising

an array of pixel sensor cells formed in a retrograde well on a substrate, wherein each pixel sensor cell has a photosensitive region, a photosensor formed on the photosensitive region, and a floating diffusion region for receiving and outputting image charge received from the photosensitive region, and

a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image; and

a processor for receiving and processing data representing the image.

71. The imager of claim 70, wherein said CMOS imager and said processor are formed on a single substrate.

72. The imager of claim 70, wherein said CMOS imager is formed on a first substrate, and said processor is formed on a second substrate.

73. The imager of claim 70, wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of the retrograde well.

74. The imager of claim 73, wherein the retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well.

75. The imager of claim 70, wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of the retrograde well.

76. The imager of claim 75, wherein the retrograde well has a dopant concentration within the range of about 1×10^{15} to 5×10^{16} atoms per cm^3 at the top of the retrograde well.

77. The imager of claim 70, wherein the retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of the retrograde well.

78. The imager of claim 77, wherein the retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of the retrograde well.

79. The imager of claim 70, wherein the retrograde well is a first retrograde well, and said circuit is formed in a second retrograde well.

80. A method of forming a photosensor for an imaging device, said method comprising the steps of:

forming a retrograde well of a first conductivity type in a substrate; and

forming a photosensor at an upper surface of the retrograde well.

81. The method of claim 80, wherein said step of forming a retrograde well is an ion implantation step.

82. The method of claim 80, wherein the first conductivity type is p-type.

83. The method of claim 82, wherein the retrograde well is doped with boron.

84. The method of claim 76, wherein the first conductivity type is n-type.

85. The method of claim 84, wherein the retrograde well is doped with a dopant selected from the group consisting of arsenic, antimony, and phosphorous.

86. The method of claim 80, wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of the retrograde well, and within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well.

87. The method of claim 80, wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to abut 1×10^{18} atoms per cm^3 at the bottom of the retrograde well, and within the range of about 1×10^{15} to 5×10^{16} atoms per cm^3 at the top of the retrograde well.

88. The method of claim 80, wherein the retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of the retrograde well, and about 5×10^{15} is atoms per cm^3 at the top of the retrograde well.

89. The method of claim 80, wherein the photosensor forming step is a photodiode sensor forming step.

90. The method of claim 80, wherein the photosensor forming step is a photoconductor forming step.

91. The method of claim 80, wherein the photosensor further comprises a transfer gate.

92. The method of claim 86, wherein the photosensor forming step is a photogate sensor forming step.

93. A method of forming a pixel sensor cell for an imaging device, said method comprising the steps of:

forming a retrograde well of a first conductivity type in a substrate;

forming a photosensitive region in the retrograde well;

forming a photosensor on an upper surface of the photosensitive region for controlling the collection of charge therein; and

forming a floating diffusion region of a second conductivity type in the retrograde well for receiving charges transferred from said photosensitive region.

94. The method of claim 93, wherein said step of forming a retrograde well is an ion implantation step.

95. The method of claim 93, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

96. The method of claim 95, wherein the retrograde well is doped with boron.

97. The method of claim 93, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

98. The method of claim 97, wherein the retrograde well is doped with a dopant selected from the group consisting of arsenic, antimony, and phosphorous.

99. The method of claim 93, wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{11} atoms per cm^3 at the bottom of the retrograde well, and within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well.

100. The method of claim 93, wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of the retrograde well, and within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of the retrograde well.

101. The method of claim 93, wherein the retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of the retrograde well, and about 5×10^{15} atoms per cm^3 at the top of the retrograde well.

102. The method of claim 93, wherein the photosensor is a photodiode sensor.

103. The method of claim 93, wherein the photosensor is a photoconductor sensor.

104. The method of claim 93, further comprising a step of forming a transfer gate on the retrograde well between the photosensor and the floating diffusion region.

105. The method of claim 104, wherein the photosensor is a photogate sensor.

106. The method of claim 93, further comprising a step of forming a reset transistor in the retrograde well for periodically resetting a charge level of the floating diffusion region, said floating diffusion region being the source of the reset transistor.

107. The method of claim 93, wherein the photosensitive region comprises a doped region of a second conductivity type.

108. A method of forming a pixel array for an imaging device, said method comprising the steps of:

forming a retrograde well of a first conductivity type in a substrate; and

forming a plurality of pixel sensor cells in the retrograde well, wherein each pixel sensor cell has a photosensitive region, a photosensor formed on the photosensitive region, and a floating diffusion region of a second conductivity type.

109. The method of claim 108, wherein said step of forming a retrograde well is an ion implantation step.

110. The method of claim 108, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

111. The method of claim 108, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

112. The method of claim 108, wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of the retrograde well, and within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well.

113. The method of claim 108, wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of the retrograde well, and within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of the retrograde well.

114. The method of claim 108, wherein the retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of the retrograde well, and about 5×10^{15} atoms per cm^3 at the top of the retrograde well.

115. The method of claim 108, wherein the photosensitive region comprises a doped region of a second conductivity type.

116. The method of claim 108, wherein the photosensor of each pixel sensor cell is a photodiode sensor.

117. The method of claim 108, wherein the photosensor of each pixel sensor cell is a photoconductor sensor.

118. The method of claim 108, further comprising a step of forming a transfer gate for each pixel sensor cell on the retrograde well between the photosensor and the floating diffusion region.

119. The method of claim 118, wherein the photosensor of each pixel sensor cell is a photogate sensor.

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